Preparation and Qualification of the Integration Site for ITk Pixel Outer Barrel Loaded Local Supports in Bonn

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I hereby declare that this thesis was formulated by myself and that no sources or tools other than those cited were used.

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CHAPTER 1

Introduction

The Large Hadron Collider (LHC) [1] at CERN is the largest and most powerful particle collider in the world and to stay at the forefront of science and technology it will be upgraded to the High Luminosity-Large Hadron Collider (HL-LHC) [2]. This is necessary to detect and precisely measure rare processes like Higgs production through vector boson fusion precision measurements.

As a result of this development the ATLAS Inner Detector (ID) [3] needs a replacement, which will be the all-silicon Inner Tracker (ITk). This detector will consist out of four layers of strip and five layers of pixel detectors and will cover the full area of the previous ID making it the largest silicon detector build to date. To build such a large silicon detector the production is spread out over multiple institutes around the world. The pixel detector is split up into three smaller subsystems, the Inner System, the Outer Barrel and the Outer Endcaps. The University of Bonn is part of this collaboration and contributes to the ITk Pixel module production and the Cell Integration step of the Outer Barrel.

To support the services and modules in the Outer Barrel so-called Local Supports will be build. These Local supports exist in two variations, the Longerons and the Inclined Half-Rings respectively. Onto these structures the Loaded Cells will be mounted with screws, which are ITk Pixel modules with a thermal interface, the Bare Cell, glued to them. These Bare Cells also serve as the mechanical connection point between Loaded Cell and Local Support. The Local supports will be mounted with Loaded Cells at the Cell Integration sites like Bonn, where about 20% of these, now called Loaded Local Supports (LLS), will be build and tested. The production process of the LLS includes many testing steps to guarantee that only functional components are further processed and no material is wasted. One testing step is the Loaded Cell reception, which is performed before the integration of the Loaded Cells on the Local Supports. Approximately 1000 Loaded Cells are expected to be tested in Bonn during the production phase. This test utilizes the Loaded Cell Quality Control (QC) Box designed by CERN to offer a common test setup for institutes involved in the Outer Barrel production. This setup is commissioned in the context of this thesis in Bonn. This test is crucial, to ensure only working ITk Pixel modules are used and to keep the need for reworks on a LLS at a low level.

To prepare, practice and qualify everything for the production of these LLS a pre-production Inclined Half-Ring is build in Bonn, for which 11 Loaded Cells need to be tested in the Loaded Cell reception. After successful testing of the Loaded Cells, the Inclined Half-Ring is assembled. The knowledge gained in this process is used to improve the testing routine for the production.

In Chapter 2 of this thesis the LHC and the upgrade to the HL-LHC will be described as well as a general introduction to the ITk and the Outer Barrel. Following this the general concept of silicon pixel

detectors is introduced with a focus on the technologies utilized in the ITk. In the next Chapter the Loaded Cell QC Box will be introduced with its working principle and the control measures to protect the devices under test (DUT). In the end a validation of these measures is shown tested with a digital ITk Pixel module. In Chapter 5 investigations in the context of a bump bond stress test are performed in collaboration with the University of Göttingen using the Loaded Cell QC Box. Here source scans, to find disconnected bumps, were performed in Bonn. In the last Chapter the construction of the pre-production Inclined Half-Ring is discussed, with a full description of the procedure and the results of the Loaded Cell reception test. In the end also a preview of the functionality of the integrated Inclined Half-Ring is shown.

CHAPTER 2

A silicon pixel detector in the HL-LHC

In this Chapter the LHC and its upgrade to the HL-LHC is introduced, as well as the upgrades too the different experiments with a focus on ATLAS and the upgrade of the ID to the ITk and its pixel detector. Afterwards the general principle of particle detection with silicon pixel detectors, consisting of the sensor, the readout processes with its corresponding readout electronic and the combination of both to a hybrid pixel module is discussed.

2.1 LHC and upgrade to HL-LHC

The LHC is located at the European Organization for Nuclear Research (CERN) in Geneva, Switzerland. The organization and the LHC are an international project with scientist from over 80 countries working on the experiments. To build the LHC the existing tunnel of the Large Electron-Positron Collider (LEP) [4], which was built in 1989 and was decommissioned in 2000, was used with a length of 27 km. The LHC was commissioned in 2009 and can accelerate bunches of protons to 14 TeV center-of-mass energy with a bunch repetition rate of 40 MHz. These protons can be collided at eight interaction points with four being used for large experiments. The experiments are: Two general purpose detectors, ATLAS [5] and CMS [6], a heavy ion focused experiment, ALICE [7] and an experiment focusing on b-physics and CP violation, LHCb [8].

To quantify a collider like the LHC usually the instantaneous Luminosity $\mathcal{L}$ is used. When integrating this quantity combined with the cross section of an interaction σ_{exp} the total number of events N_{event} can be calculated as

$$N_{\text{event}} = \sigma_{\text{exp}} \int \mathcal{L}(t)dt \tag{2.1}$$

The Luminosity for a symmetric collider like the LHC is given as $\mathcal{L} \propto \frac{N_{\text{p}}^2 n_{\text{b}} f}{4\pi F}$ with N_{p} the number of protons, n_{b} the number of bunches, F the form factor of the beam profile, including its shape and angle, and f the frequency, which results in a Luminosity of $1 \times 10^{-34}\,\text{cm}^{-2}\text{s}^{-1}$ for the LHC. This can be translated to about 1×10^9 proton-proton collisions per second. Accumulated over the lifespan of the LHC an integrated Luminosity $\mathcal{L}_{\text{int}} = \int \mathcal{L}dt$ of $260\,\text{fb}^{-1}$ is expected [9]. Even though this is already a large number of collisions it is necessary to accumulate even more data as for rare processes like the Higgs boson the cross section is very small [10] and to get a good statistical error $\sigma_{\text{stat}} \propto \frac{1}{\sqrt{N_{\text{event}}}}$ the N_{event} needs to be as high as possible.

With the current Luminosity of the LHC this is not feasible in a realistic time frame, therefore the LHC will be upgraded to the HL-LHC, which will increase the Luminosity by a factor of ~ 10 to around $\mathcal{L} \approx 1 \times 10^{-35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The increase in Luminosity results in a much higher number of collisions per bunch crossing and therefore a much higher radiation and data rate of the emerging particles. Almost all detectors at the LHC are not designed for these event rates and need to be upgraded. Research for the upgrade of the LHC and it's major experiments started in parallel to the normal operation of the accelerator including data taking at the experiments. The final construction of the upgrades is currently planned to be finished in 2029 at the end of long shutdown 3. With this upgrade the HL-LHC will stay at the forefront of research and will give interesting new insights into particle physics for decades to come.

2.1.1 The current ATLAS experiment

The ATLAS detector is the largest general purpose detector built with 45 m in length and a diameter of 25 m. It is depicted in Fig. 2.1. To fulfill the role of a general purpose detector ATLAS has multiple layers of subsystems with different particle detection techniques to gather as much information as possible from every bunch collision.

The innermost detector system is the ID, which serves the purpose of particle tracking and reconstruction of the vertices for the emerging particles. To better distinguish between the tracks of the emerging particles and measure the momentum, the ID is enclosed by a solenoid magnet system, which generates a magnetic field of 2 T inside the ID.

After the tracks of the particles are determined, their energy needs to be measured. For this purpose sampling calorimeters with different kinds of material and thickness are deployed behind the solenoid magnet. The first calorimeter of ATLAS is an electromagnetic calorimeter, which can measure the energy of light charged particles and photons. Following this is the hadronic calorimeter, which measures the energy of hadrons.

Furthest away from the interaction point is the Muon Spectrometer, which consists of several barrel layers and discs to detect the heavy, not strongly interacting Muons. For track and momentum reconstruction in the Muon Spectrometers a toroidal magnet surrounds it to bend the Muons path, which can create a magnetic field up to 4 T [9].

Inner Detector

The ID is composed out of three sub systems, the pixel detector, the Semiconductor Tracker (SCT) and the Transition Radiation Tracker (TRT) to fulfill its roll of particle tracking. A schematic view of a slice of the ID can be found in Fig. 2.2. It covers a forward angle η of 2.5 and needs to withstand the highest amount of radiation in the ATLAS detector.

The most inner system is the pixel detector, which consists out of pixel detector modules and has an area of $1.7\,\mathrm{m}^2$ of active silicon and is made up of 4 layers including the Insertable B-Layer (IBL) [12]. The innermost layer is the IBL, which is attached to the beam pipe and has pixels with a size of $50\,\mu\mathrm{m} \times 250\,\mu\mathrm{m}$. It was installed in 2014 as an addition to the existing three layers of pixel detectors. These following layers have pixels with a size of $50\,\mu\mathrm{m} \times 400\,\mu\mathrm{m}$. With all pixel layers in total a vertex resolution of almost $10\,\mu\mathrm{m}$ can be achieved.

Surrounding the pixel detector is the SCT, which is a silicon strip detector with an active area of $60\,\mathrm{m}^2$ and made up of four layers. With its silicon strip modules it is a lot more cost efficient than the pixel detector and can cover the larger area more easily, but at the loss of accuracy.

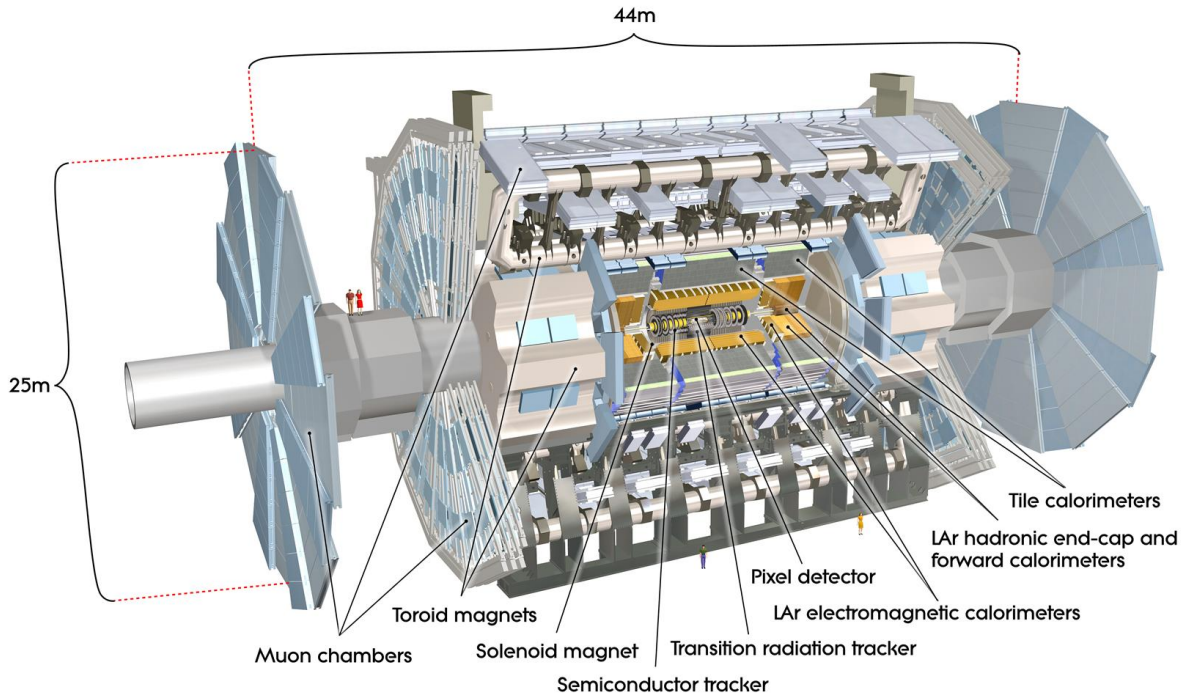


Figure 2.1: A generated image of the current ATLAS detector with its multiple subsystems.

The last part of the ID, the TRT, covers the largest area and is a gaseous straw tube detector. It has a worse single hit resolution than the other two systems, but in contrast to the silicon detectors provides much more hits per track and is cheaper to built to cover for the large area between the radius of 0.5 m and 1.1 m [3].

2.1.2 ATLAS Phase 2 Upgrade

With the HL-LHC coming up most of the ATLAS subsystems are not suitable anymore for the new environment that evolves from this upgrade. In particular the ID as the closest detector to the collision point is not suited for the higher radiation exposure and the amount of collisions created from one single bunch crossing at around one magnitude higher, than in the current LHC. While the pixel and semiconductor detector are not able to process the much higher amount of data, the transition radiation tracker would be saturated at the planned instantaneous luminosity. This would make the particle tracking almost impossible and therefore a new detector needs to be constructed. This will be the Inner Tracker (ITk), which is an all silicon detector consisting of four layers of silicon strip detectors and five layers of silicon pixel detectors, which combined will cover the whole area of the old ID as can be seen in Fig. 2.3.

Similar to the ID the other subsystems also need an upgrade, but as the scope of this thesis is the ITk Pixel Outer Barrel it will not be discussed here. Instead more information about the upgrades to the other subsystems can be found in [14].

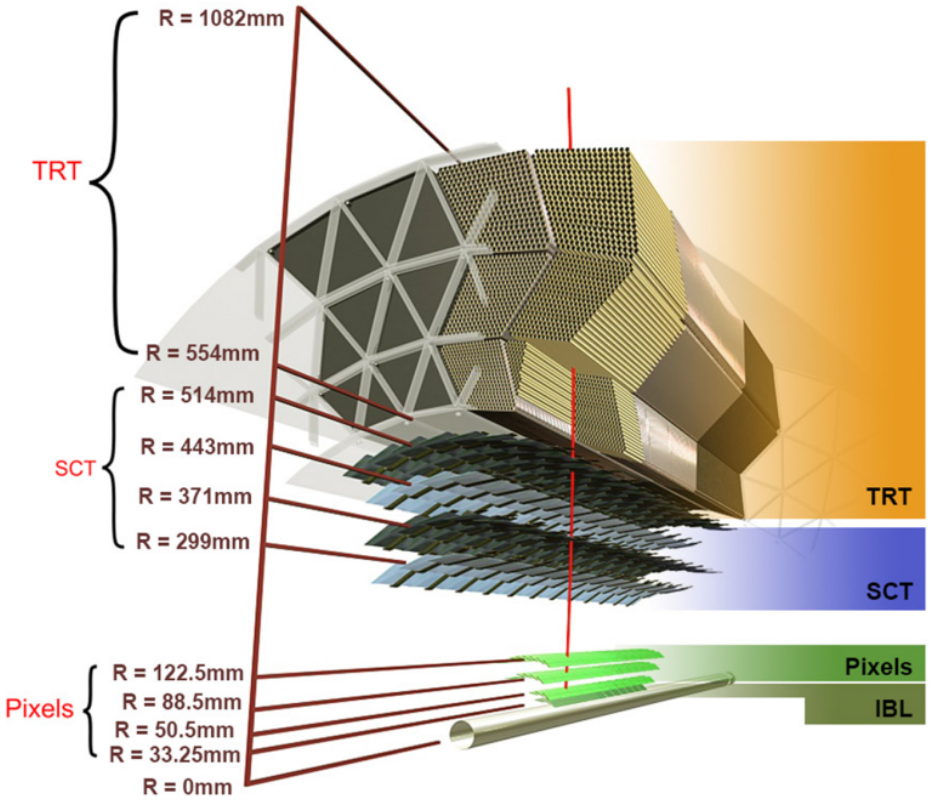


Figure 2.2: Schematic of one slice of the ID with the silicon pixel detector closest to the beam line, followed by the SCT and at last covering the most area the TRT [11].

ITk Detector

The ITk will be the largest silicon detector ever built, with its five layers of pixel detectors and four layers of strip detectors. Covering a cylindrical area up to the radius of 1.1 m and an active silicon area of 14 m^2 in pixel and 190 m^2 in strip detectors. With the upgrade the requirements for the HL-LHC will be met, i.e. for radiation hardness, data processing, material budget and a larger forward coverage up to an angle of $\eta < 4$ will be reached, while the current ID only covered up to $\eta < 2.5$.

The ITk pixel detector itself is composed out of three main systems. The Inner System, the Outer Barrel and the Outer Endcaps. These separated parts can be found in Fig. 2.4. In all of them, the ITkPix readout ASIC [15] will be used, which supports the utilized pixel sizes of 50x50 μm^2 and 25x100 μm^2. Both are significantly smaller than the pixel sizes in the existing pixel detector, with sizes between 50x400 μm^2 and 50x250 μm^2, granting a better spatial resolution and less pile up through smaller granularity, but also requiring a much higher power consumption. To compensate the larger power consumption, a serial powering scheme [16] is implemented instead of the before used parallel powering scheme. This is necessary as the cables for a parallel powering scheme would simply not fit into the available space. Also another goal of the ITk is to have a low material budget, which can only be achieved with thin ITk Pixel modules and small, thin services like the power and data cables, as well as the support structures.

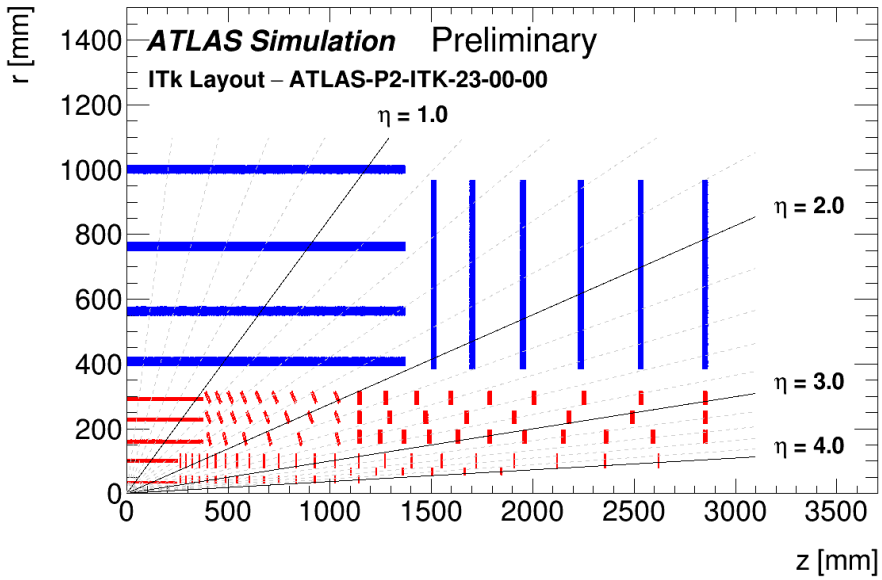


Figure 2.3: Schematic of one quatre of the cut open ATLAS ITk with the pixel detector in red and the strip detector in blue [13].

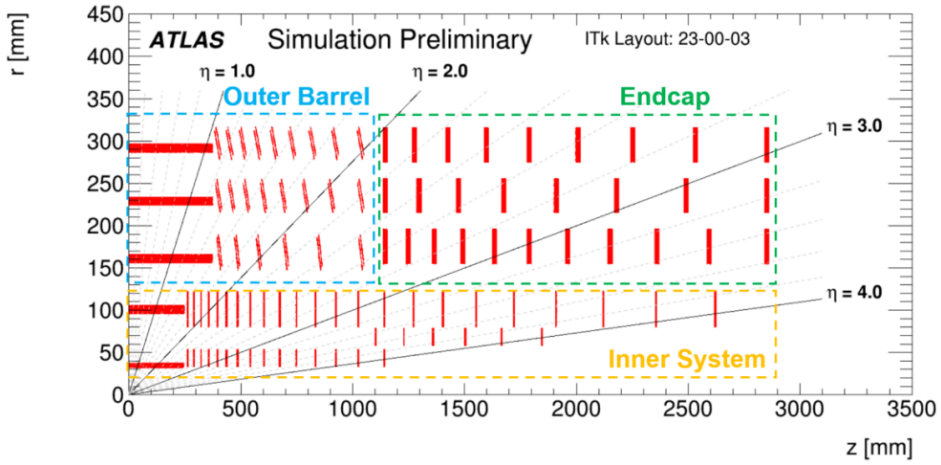


Figure 2.4: Schematic drawing of one quatre of the cut open ITk pixel detector with its three subsystem the Inner System, Outer Barrel and Outer Endcaps [13].

Most of the ITk will be built from pixel detector modules referred to as quad modules with four readout ASICs bump bonded to one sensor and a module flex. These sensors will be planar sensors, which do not have the highest radiation hardness, but are easy and cheap in production and can withstand the radiation in the outer layers. Only in the innermost layer of the Inner System triplets of three single ASIC modules will be used. Here the sensors utilized are 3D sensors, which offer a higher radiation hardness and reduced power consumption, but come at a higher production cost. Also the whole Inner System is designed to be replaced after half of the HL-LHC runtime.

In this thesis the main focus is on the ITk Pixel Outer Barrel detector, which is the largest of the three subsystems with about 50% of the 8500 quad modules.

2.2 Silicon pixel detectors

A general particle detector works by detecting the energy loss of an ionizing particle in its active volume, for silicon detectors referred to as sensor. The energy deposited in the sensor leads to the generation of free positive and negative charge carriers. If a sufficiently strong electric field is applied, the charge carriers do not recombine in the depletion region of the sensor and the drift of the charge carriers in this electric field can be measured. From here a readout ASIC needs to process the analog signal to a digital signal to store and further process it. The segmentation into layers and pixels allows for a precise measurement of the particle's tracks [17].

2.2.1 Interaction of particles in silicon trackers

Different particles interact in all kinds of ways with matter and for this reason different detectors are built. The purpose of the ITk is to measure the vertices and momentum of a particle. To achieve this the particle needs to generate a measurable signal in the silicon and should only be subjected to a small change in momentum. Most particles like uncharged particles or neutrinos do not deposit enough energy in the trackers to be measured effectively, while others like photons scatter too much, when interacting with a thicker layer of silicon. However, particles that can usually be tracked or measured in a silicon tracker are particles that ionize the detector material. The interaction of ionizing particles with matter can be categorized into charged particles and low energy photons. Both of them interact differently with matter and in the following, examples for particle interaction with silicon will be given.

Charged particles

Charged particles do interact with matter through a continuous deposit of energy in the detector layers. This energy loss can be described by the Bethe-Bloch equation [10] as given here:

$$-\left(\frac{dE}{dx}\right) = K\frac{Z}{A}\frac{z^2}{\beta^2}\left[0.5\ln\left(\frac{2m_e(c\beta\gamma)^2E_{max}}{I^2}\right) - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right] \tag{2.2}$$

with the values

- $K = 4\pi N_A r_e^2 m_e c^2 = 0.307\,\mathrm{MeVcm^2mol^{-1}}$ with the electron mass and radius,
- Z the atomic number and A the mass number of the penetrated target material,
- z the charge and β the velocity of the incident particle
- $E_{max} \approx 2m_e(c\beta\gamma)^2$,
- I the mean excitation energy of the target material, in this case silicon with $I = 173eV$,
- $\delta(\beta\gamma)$ the density correction factor.

This equation describes the energy deposit of the incident particle of $0.1 < \beta\gamma < 1000$ within a few percent accuracy. Particles with about $\beta\gamma \approx 3$ and above are considered minimum ionizing particles (MIP) until $\beta\gamma \approx 1000$, because as can be seen in Fig. 2.5 the energy deposit does only increase slightly from the minimum [10]. Therefore an energy loss for silicon in this region can be approximated to $\left(\frac{dE}{dx}\right)_{\text{Si}} = 3.87\,\text{MeV}\text{cm}^{-1}$ [17].

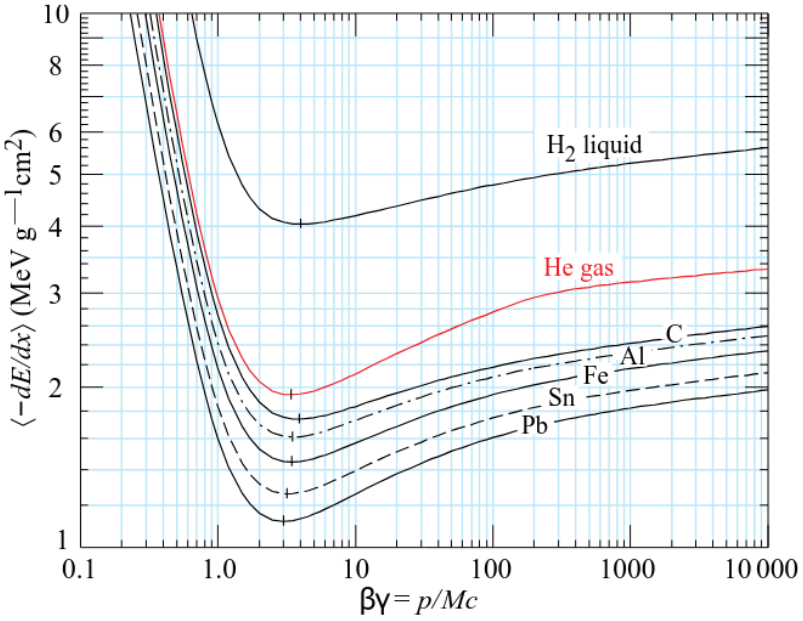


Figure 2.5: Mean energy loss of heavy charged particles in matter derived from Eq. (2.2) with $\beta\gamma$ as energy of the traversing particles energy [10].

For charged particles that are undistinguishable with a low mass and relativistic energies above $\beta\gamma \approx 1000$ effects like bremsstrahlung start to dominate and the Bethe Bloch equation is not accurate anymore. To calculate the energy loss for bremsstrahlung the equation

$$-\left(\frac{dE}{dx}\right)_{\text{brems}} = \frac{E}{X_0} \tag{2.3}$$

with the radiation length X_0 is used, which is the mean length the particle needs to travel through the material to reduce its energy to $\frac{1}{e}$. For silicon the radiation length is about $X_0 = 9.36\,\text{cm}$ [17], which is large compared to the typical thickness of the active layer of a silicon pixel or strip detector at about 100–500 μm.

Photons

For photons the three dominating effects that lead to ionization are the photoelectric effect, Compton scattering and pair production. The photoelectric effect as well as pair production result in the full absorption of the photon in the silicon sensor, while the Compton effect results in a scattering of the photon [18]. The interaction probability of these processes is energy dependent and can be seen

in Fig. 2.6. In general a silicon detector at large experiments like ATLAS is not primarily used to detect photons, but particles that leave tracks through multiple layers of silicon detectors. Scattering or absorption of photons is an unwanted side effect, that can be minimized by less material in the path of the photon.

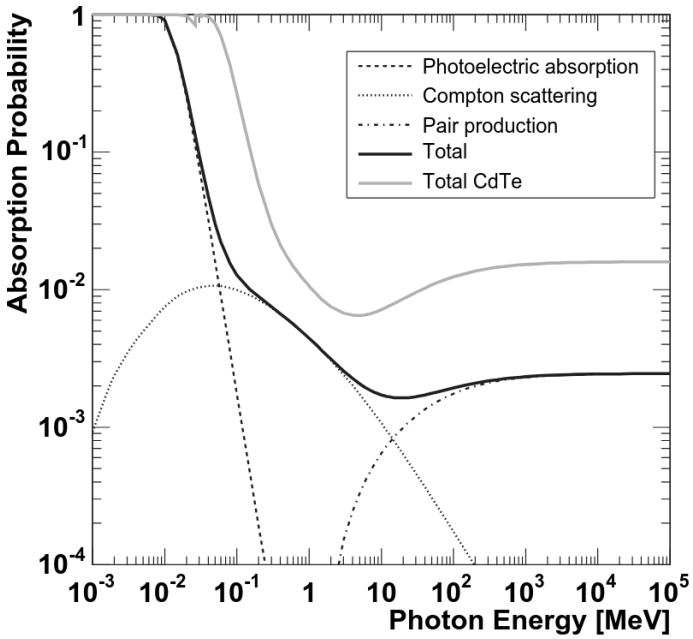


Figure 2.6: Absorption probability for photons with different energies in silicon depending on the different photon interactions with matter [18].

2.2.2 Particle detection

The signal of a silicon pixel detector is generated in the depletion region of the sensor. To create this region a weakly doped n- or p-type silicon is used as a bulk and a strongly opposite type doped silicon is used as a readout electrode. This combination leads to a large depletion zone in the bulk, which grows even bigger, when a reverse bias voltage is applied. The sensor itself can be approximated as a diode in reverse bias. This gives a typical diode IV curve, which is characterized by a small leakage current and a breakdown voltage. The leakage current is the current flow through the sensor, when the reverse bias voltage is applied. With a growing depletion zone, the leakage current slowly increases until the point, where the sensor volume is fully depleted and the leakage current saturates. At some point the reverse bias will be high enough to reach the breakdown voltage. Then the leakage current starts to rapidly increase, which typically leads to irreversible damage to the sensor.

As described in Section 2.2.1 particles traversing matter will interact with it in different ways, but all detectable particles ionize matter. To create free charge carriers, the deposited energy of the ionizing particle in silicon needs to be on average about $E_{\text{creation}} = 3.65\,\text{eV}$ [17]. With this value the number of charge carriers, N_e^- and N_h created by a traversing particle, can be calculated by $N_e{}^- N_h = \frac{E_{\text{deposite}}}{E_{\text{creation}}}$. Without an electric field these free charge carriers would recombine, but in the depletion region of a silicon sensor these free charge carriers drift in the strong electric field towards the readout electrodes.

These drift will then induce a charge in the readout electrode, which can be measured and processed by each pixels signal processing electrode.

2.2.3 Signal processing

The readout process of a pixel electrode is shown in Fig. 2.7. Each pixel has its own readout circuit and the charge induced from the sensor is first processed by a Charge Sensitive Amplifier (CSA). This component integrates over the input charge and transforms it into a voltage pulse with the amplitude being proportional to the integrated input charge. In this example a constant current is used to reduce the collected charge at the CSA input, which is called feedback. This causes a linear falling edge in the resulting voltage pulse and with a sufficiently steep rising edge, the width of the voltage pulse is proportional to the integrated charge. The CSA is followed by a discriminator to convert the analog voltage pulse into a digital signal. To do so the analog signal is compared to a threshold voltage: If the incoming signal is higher than the threshold the discriminator output corresponds to a high logic level. For analog signals lower than the threshold, the discriminator outputs a logic low. As the width of the voltage pulse is proportional to the charge the Time over Threshold (ToT) is proportional to the amplitude of the signal and can be used as a measure of energy deposited in the sensor.

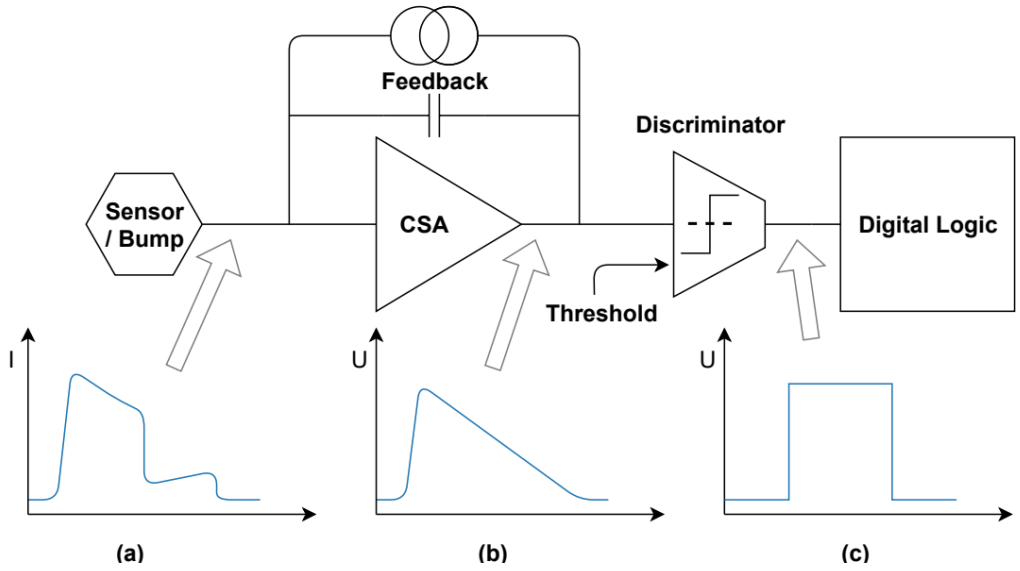


Figure 2.7: Electronic circuit of a standard pixel detector. The signal from the sensor is a current pulse (a), which is than transformed into a voltage pulse by the CSA (b) and in the end digitized by the discriminator (c) [19].

In an ideal case the response of the discriminator would be a step function, but due to electrical noise the response is closer to a s-curve, shown in Fig. 2.8. It can be described by:

$$P(Q) = 1 - \mathrm{erf}\left(\frac{Q-\mu}{\sigma\sqrt{2}}\right) \tag{2.4}$$

with $P(Q)$ the probability for a charge inserted into the analog circuit and afterwards resulting in a high output of the discriminator, μ the threshold and σ the noise of readout circuit [17]. Through this

definition the threshold of the discriminator is the charge Q that results in 50% hits detected by the discriminator and the noise is the width of the s-curve, which is one standard deviation.

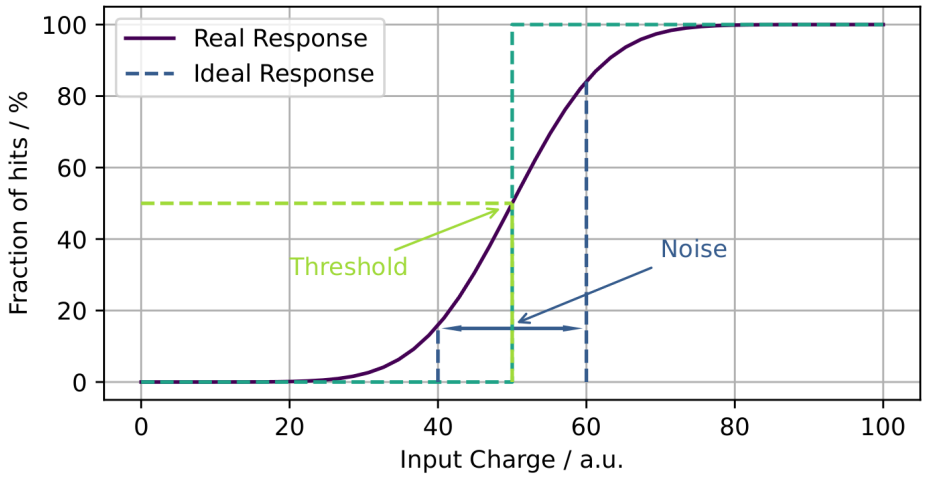


Figure 2.8: An example plot for an ideal and a real s-curve of a pixel on an silicon pixel detector with the fraction of hits detected plotted against the input charge [20].

2.2.4 Hybrid pixel modules

Many pixel detectors, like the ITk pixel detector, utilize hybrid pixel modules as a base building block. A general schematic for such a module is shown in Fig. 2.9. This detector module consists out of a silicon sensor and one or more silicon readout ASICs which are bump bonded to the sensor. This process of bump bonding is rather expensive as modern pixel sizes are only a few μm^2 large and number in the 1×10^6 per hybrid module. Nevertheless designing and optimizing the sensor and the readout ASIC on their own makes them more flexible and suited for their specific task, allowing for optimized processes.

In the figure also the wire bonds are indicated, which are the power and signal connections for the hybrid pixel detector. These wire bonds usually connect to a thin Printed Circuit Board (PCB), called module flex, which has connections and routes for the powering and further signal processing. Depending on the structure of the hybrid pixel module the module flex is glued to the sensor backside or the readout ASIC.

An effect that can occur with a lot of pixel readout electronics in such close vicinity, as on a hybrid pixel module, is cross talk. This effect occurs, when the readout electronics of a pixel detect a signal, that occurred in a neighboring pixel. Such a connection can occur through capacitive coupling between the pixel readout electronics, when the input charge is high above the threshold. Either through the pixel implantation in the sensor or to a lesser extend in the substrate of the readout chip [19].

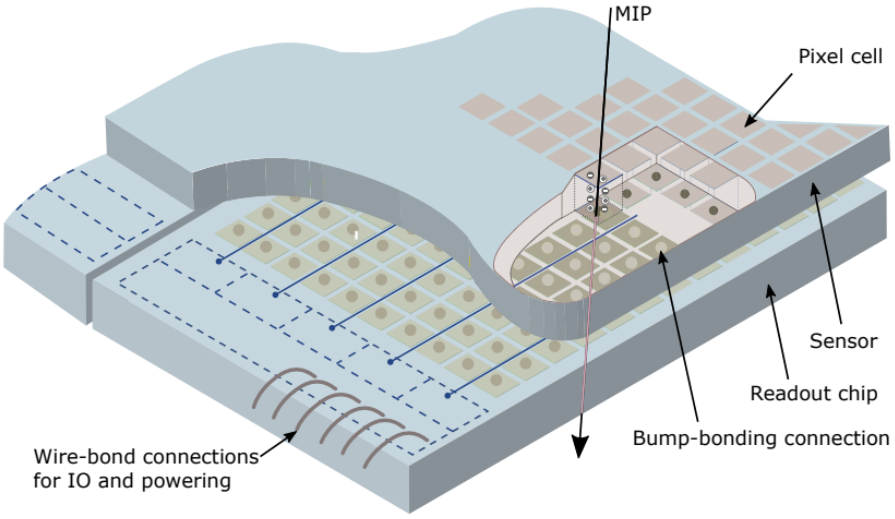


Figure 2.9: A schematic of a hybrid pixel module with the sensor and its pixels on top and the readout ASIC bump bonded to it. Also a MIP is shown traversing the hybrid pixel module [21].

CHAPTER 3

The ITk Outer Barrel

The University of Bonn is one of the Cell Integration sites of the ITk Outer Barrel. To clear up the different nomenclatures and the key components of the Outer Barrel a full built up, started from the readout ASIC, to the ITk Pixel module and the Local Support structures is described in this chapter. Also the different steps and testings throughout the production of the Outer Barrel will be explained.

3.1 The ITkPix readout ASIC

The readout ASIC used for the ITk pixel detector is the ITkPix [15]. It was designed by the RD53 Collaboration, which was formed in 2013 and had the goal to develop the readout ASICs for ATLAS and CMS. The ITkPix readout ASIC exists in three versions, the ITkPixV1, ITkPixV1.1 and ITkPixV2, of which only the ITkPixV1.1, build on the RD53B design library and the ITkPixV2, build on the RD53C design library are relevant for this thesis. The ITkPixV1.1 is the readout ASIC used for the pre-production and testing and is the only in this thesis tested readout ASIC, while the ITkPixV2 will be used in the production of the ITk.

The ASIC is built on a 65 nm CMOS process by TSMC and can withstand the high radiation levels in the ITk with a low power consumption. It supports the different pixel pitches required in the ITk pixel detector. The ITkPix readout chip consists of a pixel matrix and a chip bottom. The pixel matrix is built from identical cores of 8×8 pixels of 50x50 μm^2 size. The complete matrix consists of 400×384 pixels, or 50×48 cores, totaling in 153600 pixels per readout ASIC. The chip bottom contains wirebond pads and all system functionality, e.g. power management, monitoring and data transmission. This data transmission utilizes differential signals. Each chip offers 4 uplinks (up to 1.28 $\frac{\text{GBit}}{\text{s}}$ each) to send data and one downlink (typically 0.16 $\frac{\text{GBit}}{\text{s}}$) to receive data. In addition a four data input lanes for data merging and four general purpose outputs.

The readout logic is similar to the standard signal processing described in Section 2.2.3, with the analog front-end (a) and the digital pixel logic (b) shown in Fig. 3.1. Here the different components can be found, like the CSA and the comparator in the analog part, as well as the pad for test injections into the analog front end. Similar to that, in the digital part the comparator, the different enable bits and the digital injection point can be found. Also the HitOr logic is shown. The HitOr is a logic OR of all comparator outputs and outputs a high logic level if at least one comparator outputs a high logic level. This HitOr output can be used to trigger a matrix readout, which is utilized for the self trigger scan

described in Section 3.2.1.

3.2 ITk Pixel module

The most fundamental building block of the ITk Pixel Outer Barrel detector is the quad module, in this thesis referred to as the ITk Pixel module. The quad module is a hybrid pixel detector, consisting of four readout ASICs, the ITkPix, bump bonded to a single sensor tile, called a Module Assembly. The sensor backside of this Module Assembly is then glued to a flexible PCB, the module flex. It is electrically connected to the Module Assembly using thin wire-bonds. To protect the wire-bonds, a mechanical wire-bond protection is glued to the pick-up points on the module flex, which can be found in Fig. 3.2. Here the counter clockwise numbering of the readout ASICs is shown and the pick-up points are marked. With four ITkPix readout ASICs the ITk Pixel module has in total 614400 pixels. Only between the edges of the readout ASICs two rows of double sized pixels exist to cover the space between the readout ASICs. Also the data and power connectors are shown, where specialized pigtails are connected to readout and power the ITk Pixel module.

While each readout ASIC offers up to four uplinks, each quad module in the Outer Barrel only requires up to two uplinks for the full module. This is possible due to the process called data merging, which allows a single readout ASIC to receive data from other readout ASICs and merge the data streams internally. The combined data is then sent out using one (Layer 3 and Layer 4) or two (Layer 2) uplinks.

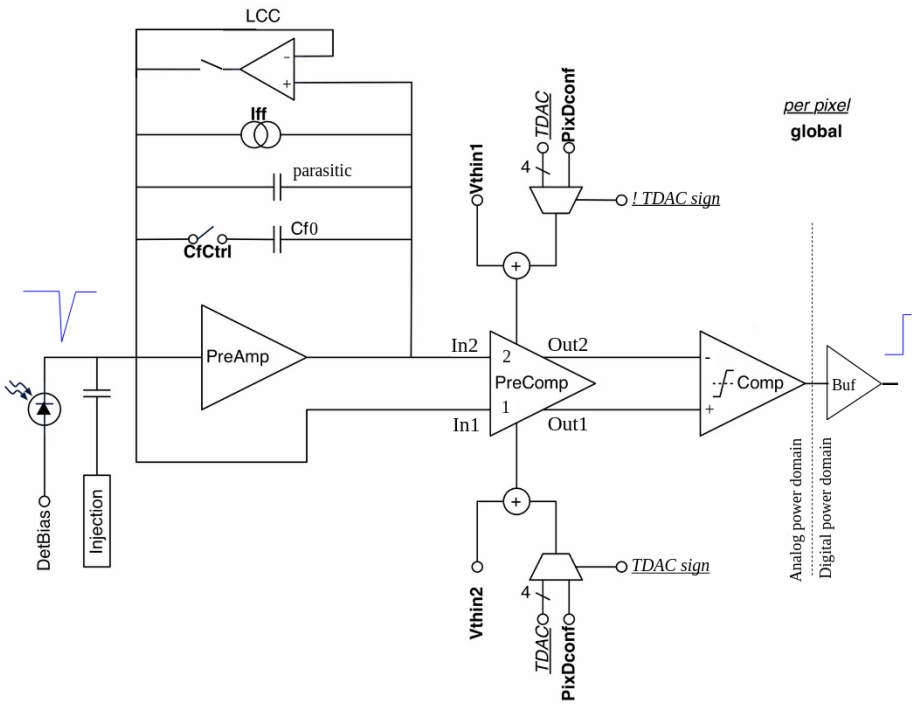
In the Outer Barrel each Module Assembly is glued on a Bare Cell, forming a Loaded Cell shown in Fig. 3.3 (a). These Bare Cells consist of a Pyrolytic Graphite Tile (PGT) and a Cooling Block, as shown in Fig. 3.3 (b). The main purpose of the Bare Cell is to provide a mechanical connection point and thermal interface for the ITk Pixel module. The PGT offers a large thermal conductivity of $2\,000\,\mathrm{Wm^{-1}K^{-1}}$ in the transverse direction, while the Cooling Block is well suited for conducting heat in the Z-direction with a thermal conductivity of $180\,\mathrm{Wm^{-1}K^{-1}}$, comparable to aluminum at a reduced material budget [22].

3.2.1 Readout of the ITk Pixel module with BDAQ

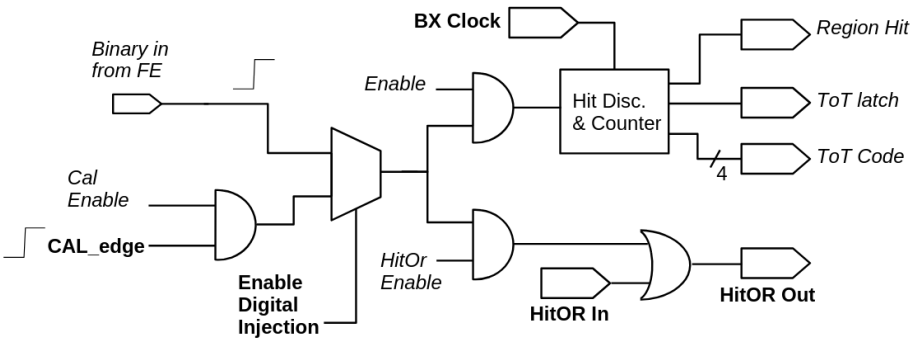
To process the data of the four ITkPix readout ASICs on an ITk Pixel module a dedicated readout system needs to be deployed. There are two systems in use, which are BDAQ [23] and YARR [24]. While BDAQ is a Python based readout system and developed in Bonn, YARR is C++ based. Most scans in Bonn are performed with BDAQ and are comparable to the YARR counterpart. In the following a short overview of some standard scans are shown and in the end standard failure criteria used in the ITk Pixel module production for these scans are shown.

Digital scan

A digital scan provides information about the functionality of the digital hit processing of the readout electronics of the ITkPix readout ASIC [15]. To do so, a certain number of test injections in the digital part of each pixel is performed and is compared to the number of detected hits.



(a)



(b)

Figure 3.1: Analog front-end (a) and digital pixel logic (b) of the ITkPix readout ASIC [15].

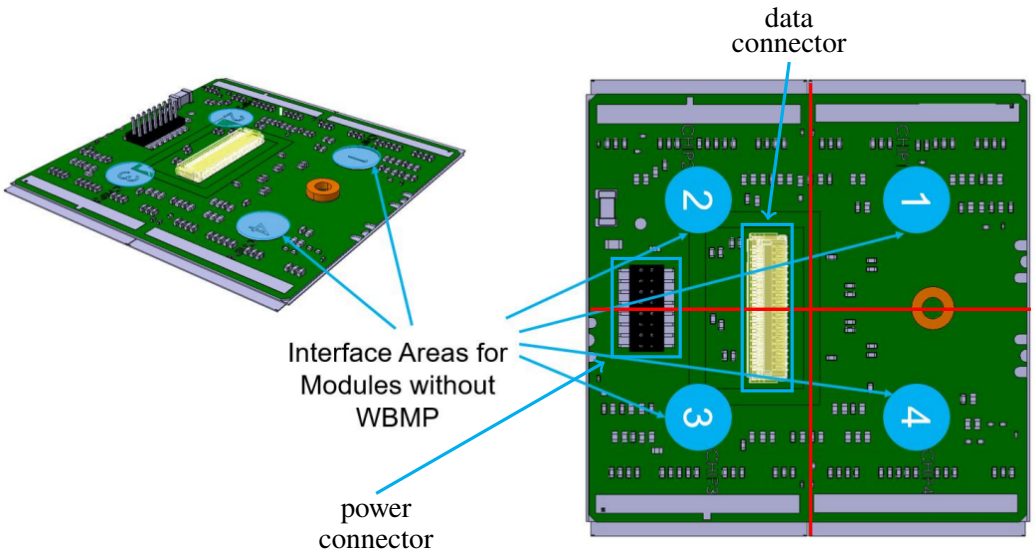


Figure 3.2: The module flex marked at the four pick-up/glue points for the wire-bond mechanical protection (WBMP) called interface areas and separated into the four readout ASICs by the red lines. The numbers on the pick up points also correspond to the numbers assigned to the readout ASICs [22].

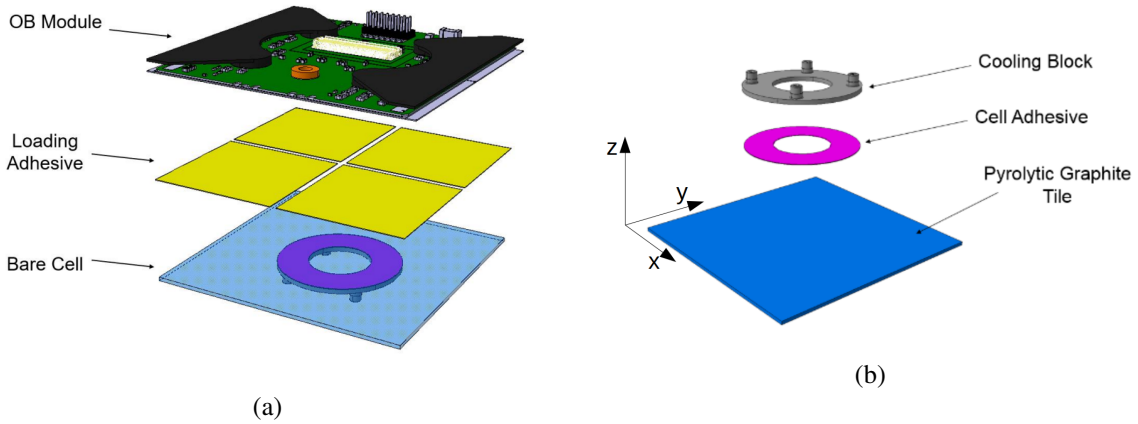


Figure 3.3: Schematics of the Loaded Cell composed out of the Bare Cell and the OB Module (a) and the Bare Cell itself disassembled in the Cooling Block, Glue and Pyrolytic Graphite Tile (b).

Analog scan

An analog scan is similar to a digital scan, but the pulses are injected into the analog readout electronics of the ITkPix readout ASIC. Similar to the digital scan, the figure of merit is the number of recorded hits per pixel compared to the number of injections per pixel.

Global and local tuning of the threshold

The threshold of a pixel is defined as in Section 2.2.2. For a given comparator threshold setting, each pixel response will be slightly different due to process variations. Therefore a tuning of the threshold is necessary, to acquire a similar signal response from all pixels when injected with the same charge. To tune the pixels on the ITkPix a 5 bit register per pixel, called TDAC and a global threshold register of 10 bits, called GDAC, is available. While the GDAC offers range, the TDAC offers per pixel precision. The optimal GDAC value is determined as the GDAC setting, for which the mean occupancy for the full matrix is closest to 50% of the total number of injections. During GDAC tuning the TDACs for each pixel are set to a centered value. After finding the optimal global threshold setting, the TDAC setting is varied for each pixel such that the per pixel occupancy is closest to 50% of the number of injections per pixel.

Threshold scan

In a threshold scan multiple analog injections with rising charges are carried out in each pixel. From this a s-curve is measured for every pixel, which looks like the s-curve in Section 2.2.2.

From each s-curve a threshold and noise can be calculated and formed into a distribution for all pixels on a ITkPix readout ASIC. This distribution is gaussian and a fit can be applied to it. This can be used to determine a mean and standard deviation of both threshold and noise. As these values are easily affected by changes to the ITk Pixel module and its environment as every pixel is measured multiple times, they are often used to compare a module in different steps of production.

Noise occupancy scan

The goal of a noise occupancy scan is to find pixels that have a high discriminator output without an injection or a hit. Such pixels can be found by running a scan with many triggers, but without any injections. A typical threshold to designate a pixel as noisy is $n_{\text{threshold}} = 10 \times 10^{-6}$, meaning on average one in 10×10^{6} triggers would result in the detection of a hit by the pixel despite no injection into the readout circuit. To account for external sources, like cosmic radiation, this scan typically is performed with at least 10×10^{7} triggers.

Self trigger scan

A self trigger scan is an efficient approach for measurements with radioactive sources to ensure proper timing for trigger signals. To this end, the HitOr circuit of the ITkPix is used to trigger the readout of the full matrix. This way a matrix readout is triggered by the readout chip itself, whenever any one pixel detects a hit.

Stuck pixel scan

This scan identifies stuck pixels, which are pixels that have an output that is effectively always high. As the readout logic only detects rising or falling edges, it will usually just be identified as a dead pixel. Nevertheless such pixels need to be deactivated to run self trigger scans, as these scans relay on the HitOr and if one pixel is always high, the HitOr input would be always high for all other pixels, rendering

the HitOr useless. To still identify these pixels an initializing first rising edge is forced to get the stuck pixel into the always high state, which is detectable and can then be deactivated.

Disconnected bump scan

For a disconnected bump scan an injection pattern in a ring around the tested pixel is used, visible in Fig. 3.4. An injection charge an order of magnitude higher then the threshold is chosen, which leads to cross talk between the pixels through the sensor and readout ASIC. This effect is explained in Section 2.2.4. In case the bump is not connected to the sensor no cross talk occurs, because the largest source of cross talk, the sensor, is not connected and the injection into the surrounding pixels is not detectable by the pixel in the middle. To account for bad connections all pixels with 50% less hits, than injected into the surrounding pixels, will be masked.

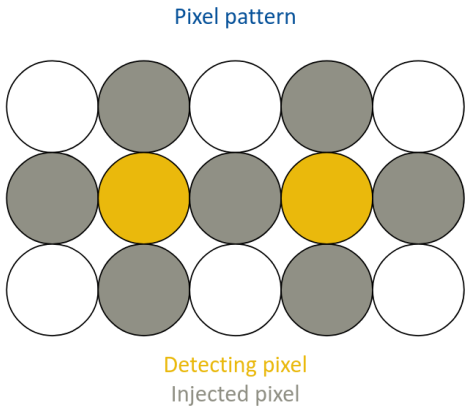


Figure 3.4: Injection pattern used in a disconnected and merged bump scan.

Another method to measure a disconnected bump is a self trigger source scan. Here the module gets placed under a source for an extended period of time, after which it will detect a high number of hits. Ideally all disconnected bumps would detect no hits, but some pixels are just badly connected and also need to be masked, as they do not reliably detect hits. Nevertheless it also needs to be accounted for SMDs or other objects, that could block radiation. A proven cutoff criteria is to consider pixels with less than 5% of the mean occupancy as disconnected.

Merged bump scan

A merged bump scan is designed to find merged bumps. It works by means of crosstalk, similar to the disconnected bump scan, but with an injection charge similar to the threshold. This injection charge does generally not lead to crosstalk hits in a neighboring pixel and therefore after injection no hits should be detected by the tested pixel. If nevertheless the pixel detects hits, it can be explained by a merged bump, but also noise or a cosmic particle could lead to such a detection. To account for this only pixels with more then 50% detected hits of the injections into the neighboring pixels are considered merged and consequently masked.

Failure criteria for the standard scan routine

In Table 3.1 the typical values are shown for a pixel to fail in one of the above mentioned scans during a standard scan for a ITkPix in the Outer Barrel [25].

Scan type	No. and type of injection	Injection charge	Pixel pass criteria in No. of detected injections
Digital	100 digital injections in pixel	High signal	100 ± 2
Analog	100 analog injections in pixel	10 000 e^-	100 ± 2
Merged bump	100 analog injections in cross around pixel	2 000 e^-	0 - 50
Disconnected bump cross talk	100 analog injections in cross around pixel	35 000 e^-	50 - 102
Disconnected bump source scan	from source	Self trigger with source	5% of the mean occupancy
S-curve	Multiple analog scans		If s-curve fit fails

Table 3.1: The criteria for a pixel to pass in the standard ITk Pixel module scan routine with the ITk Pixel module tuned to 1 500 e^-.

3.3 Outer barrel support structures

The Outer Barrel consists of a barrel section and an inclined section, both with dedicated support structures. Schematic drawings of both flavors of Functional Local Supports, so Bare Local Supports with Cooling Pipes and Base Blocks attached, are shown in Fig. 3.5 and Fig. 3.6. Local supports for the barrel section are referred to as Longerons and the inclined section consists of Inclined Half-Rings, often referred to as just Half-Rings. All information in this Section come from the design report, which can be found on EDMS [22].

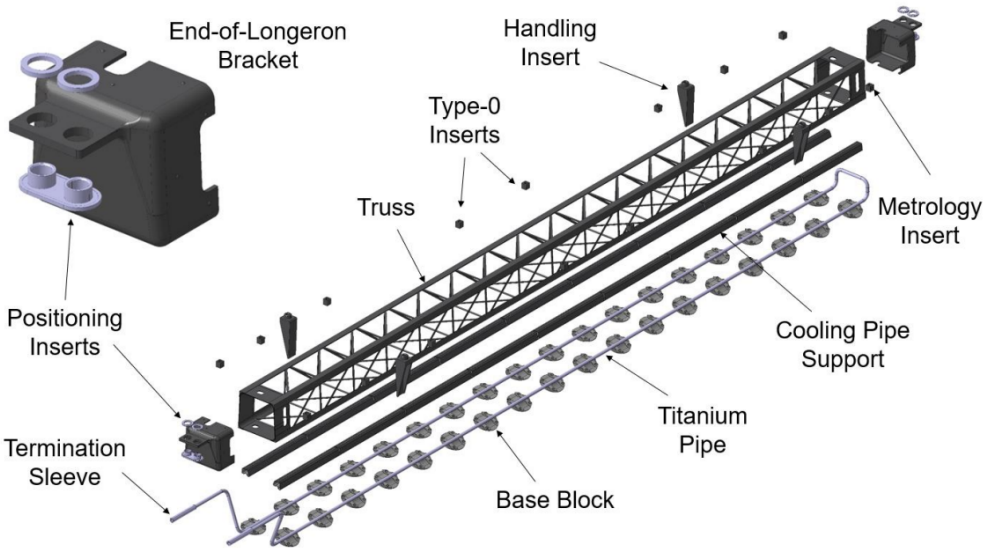


Figure 3.5: Schematic drawing of a functional longeron separated into its main components [22].

The carbon truss of the Functional Local Supports is strong enough to support the ITk Pixel modules the cooling and the services, with minimal bending of the whole structure. It is even strong enough to support a small sized physicist, while offering one of the smallest material budgets possible.

In general all Longerons follow the same schematic and are 750 mm long. The Inclined Half-Rings need to have different sizes depending on their position, therefore there are Layer 2, 3 and 4, with Layer 2 having a diameter of 160 mm, followed by Layer 3 with 228 mm and at last Layer 4 with 288 mm.

On the Functional Local Support, Base Blocks are welded to the Cooling Pipe. The ITk Pixel modules are mounted on the Base Blocks using screws, which allows for reworking of the Local Support in case of a failure of one ITk Pixel module. To connect the ITk Pixel modules to data transition and power cables, dedicated PCBs, referred to as PP0s, are installed on top of a Longeron and besides an Inclined Half-Ring. Fig. 3.7 and Fig. 3.8 show example CAD drawings of a Longeron and an Inclined Half-Ring with PP0. Each PP0 corresponds to one serial powering chain, also called SP chains, in the detector. Through these SP chains 6.25 A are supplied to each ITk Pixel module and each ITk Pixel module on the SP chain has a voltage drop of about 1.6 V. This results in an absolute voltage at the first ITk Pixel module of $\sim$ 1.6 V times the number of ITk Pixel modules, while the second one sees a voltage of $\sim$ 1.6 V time the number of ITk Pixel modules minus one. In addition to the SP chain on each PP0, one or two high voltage chains are installed to reverse bias the sensors of each ITk Pixel module. These HV

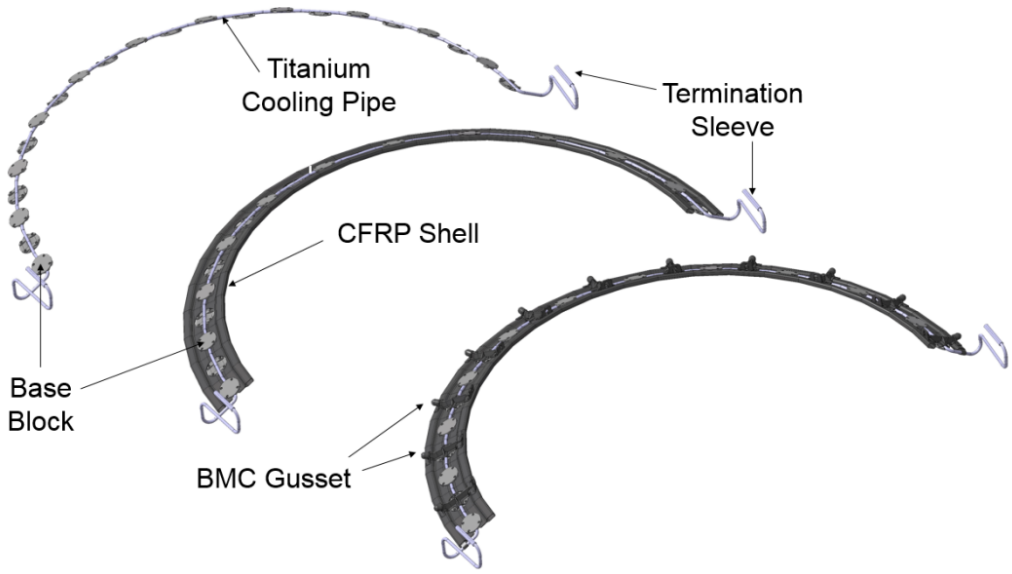


Figure 3.6: Schematic drawing of a functional Half-Ring for Layer 3 separated into its main components [22].

chain power the ITk Pixel modules sensor in parallel and are referenced to the low voltage of the the ITk Pixel module it biases, which can lead to large differences between the bias voltages over a whole SP chain.

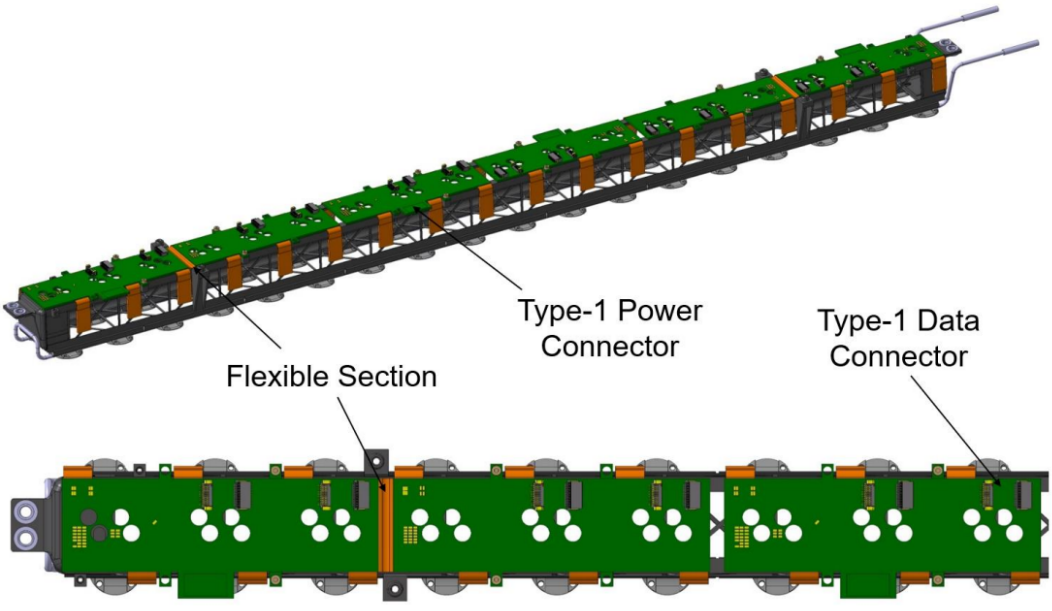


Figure 3.7: CAD drawing of four PP0s on the Longeron with different kinds of PP0s connected [22].

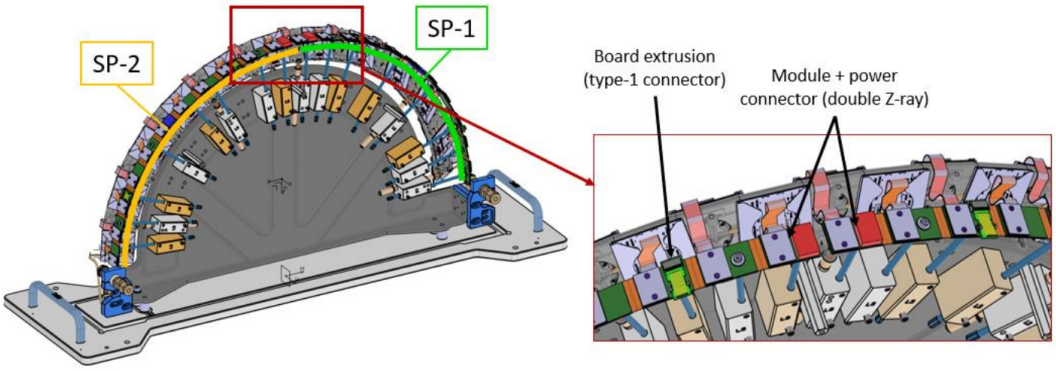


Figure 3.8: An example simulation for the two SP chains on a Layer 3 Inclined Half-Ring [22].

To finally connect the ITk Pixel modules and the PP0 a pigtail is used. This pigtail comes in different variations for the Longeron and Inclined Half-Ring and they are shown in Fig. 3.9, where they are already connected to an ITk Pixel modules. For a good electrical connection, an interposer with small spring contacts is placed between the pigtail and the PP0 before screwing them together. This is shown in Fig. 3.10. When all ITk Pixel modules are connected to the PP0 and the Functional Local Support it is

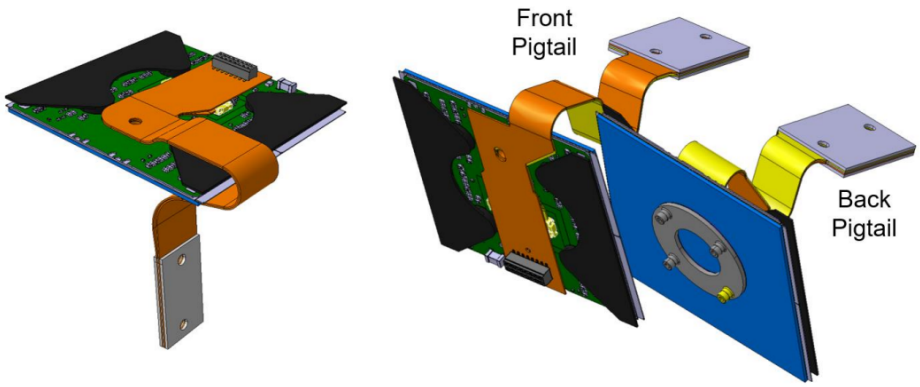


Figure 3.9: The CAD drawing of the three different types of pigtails. One type for the Longeron and two separate types for the front- and backside of the Inclined Inclined Half-Ring [22].

referred to as a LLS. Multiple of these LLS will then be installed to create one layer of the Outer Barrel shown in Fig. 3.11.

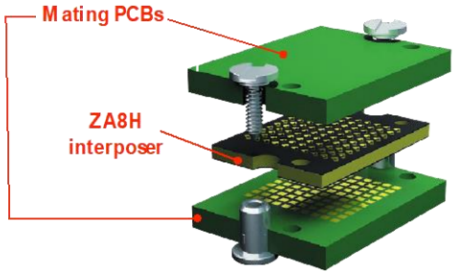


Figure 3.10: Drawing of the connection between the PP0 and the pigtail PCBs with an interposer in between [22].

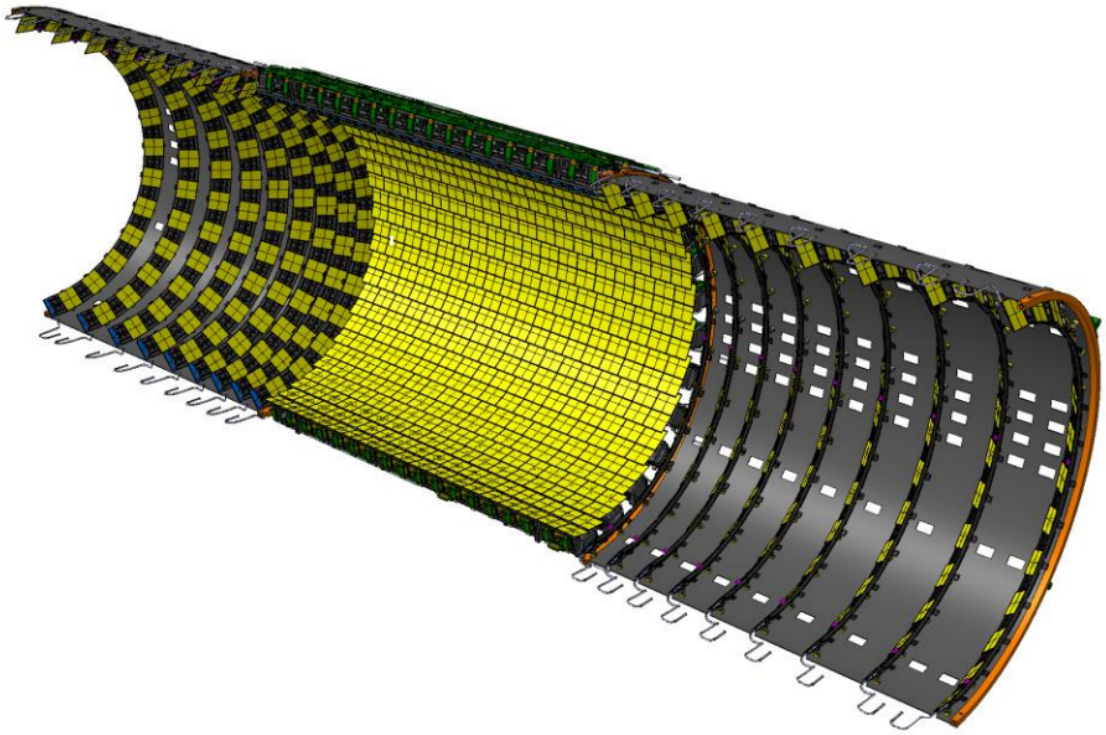


Figure 3.11: CAD drawing of half a Layer 4 of the Outer Barrel with Longeron and Inclined Half-Rings installed [22].

3.4 Production of the ITk pixel detector

To built the largest pixel detector in history multiple institutes over the globe have to participate and work together in multiple different production areas and groups. For example the production the later introduced pre-production Half-Ring for the ITk Pixel Outer Barrel is be done by institutes from France, Japan, Germany and Switzerland, as well as CERN, in close collaboration. Because of this it is important

to establish standard production procedures, transport methods and a production database in order to guarantee a homogeneous, good quality of all components.

To create and test these necessary processes a pre-production is initiated after the technical design of the components is mostly finished. In this pre-production all different processes are carried out with a certain number of parts to guarantee a satisfactory quality of production parts from all sites. To store all the created data from the different testing stages a production database [26] will be implemented in the production. This production database dictates the serial numbers for the different components and links them together. For the pre-production this database was not ready and different approaches and storing methods are used.

Production flow

In this production flow only the important steps after the production of the Module Assembly and towards the assembly of the LLS will be discussed. This production flow can be found in Fig. 3.12, where the different steps and shipments are shown.

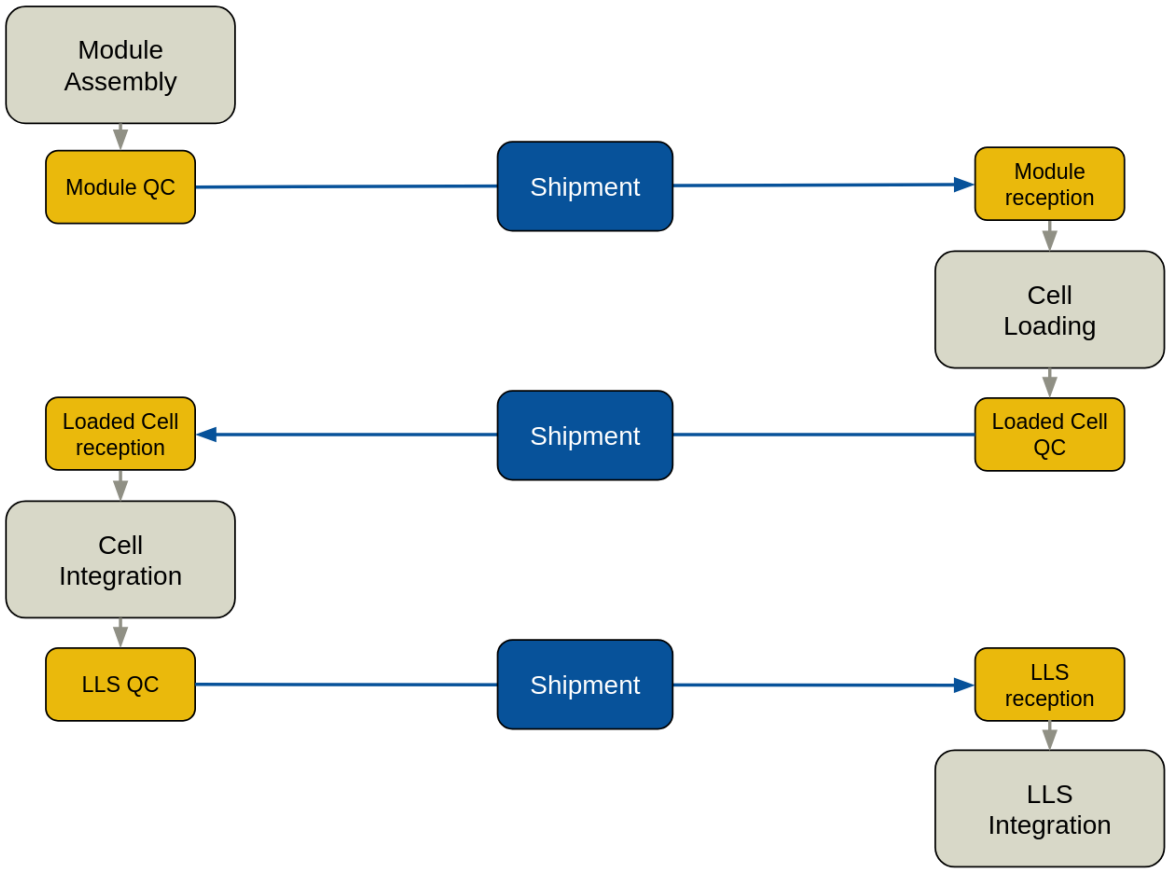


Figure 3.12: The production flow of a Module Assembly to a LLS with its different steps and testing stages, as well as the shipments in between.

The first step, after the assembly of a Module Assembly at a module production site, is the Module Quality Control (Module QC). Here different physical and electrical tests for the module flex, sensor and

readout are carried out. These tests determine if the Module Assembly meets the standards for a further production and create a configuration for the Module Assembly. That configuration is then used at the other testing sites to run similar scans for a comparison.

After a Module Assembly passed the Module QC it will be shipped to a Cell Loading site. Here a slimmed down test cycle looks for transport damages by utilizing the configuration created in the Module QC and comparing the Module Assembly to the Module QC data. If the Module Assembly is still in a good condition it will be glued to a Bare Cell. To ensure this process did not damage the now Loaded Cell, a more thorough testing cycle is carried out similar to the Module QC, called the Loaded Cell QC. For most Outer Barrel ITk Pixel modules, the production of the Module Assembly and the Loaded Cell are two separate steps. However, in Japan Loaded Cells are produced in a single production step from the Bare Modules, skipping the Loaded Cell QC as a testing step.

From the Cell Loading site the Loaded Cell is shipped to a Cell Integration site like Bonn. Similar to the Cell Loading site a shortened test routine after transport, the Loaded Cell reception, is carried out to check if the Loaded Cell is performing as expected. If so the pigtail installation and integration of the Loaded Cell on a Functional Local Support starts. Again in the end a full electrical test on the LLS is done in the LLS QC, as this is the last step where a re-work of the LLS is possible. The fully integrated LLS is then shipped to CERN, where it is stored until the construction of the Outer Barrel.

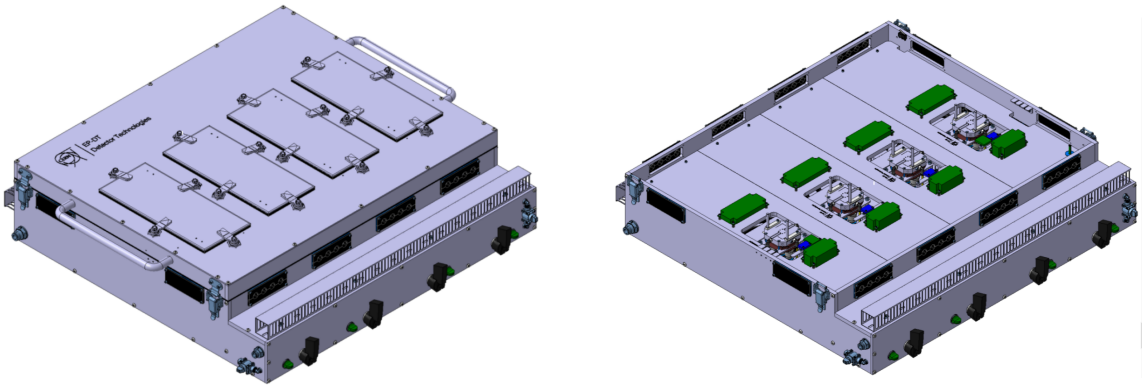
All of these test cycles on the ITk Pixel module are carried out to minimize the waste of material and to keep the need for re-works on a minimal level. Also some of the shipments between sites are difficult, for example from the already mentioned Module Production site in Japan to any Cell Integration site, that are all located in central Europe, making it necessary to check for transport damages.

CHAPTER 4

Loaded Cell QC Box

As discussed in the previous chapter, the ITk Pixel modules will be tested between each production step. This ensure that only modules that meet all quality criteria for the final detector are installed and keeps the need for re-working ITk Pixel modules at a minimum. While an in-depth characterization of each ITk Pixel module is only done after the Module Assembly and Cell Loading, simplified reception tests are conducted at each subsequent step in the production cycle, with the goal to catch potential damages that occurred during handling or transport to an ITk Pixel module and remove it from the production chain. In order to provide comparable test conditions at the various stages in the cycle of an ITk Pixel module prior to the integration on a Functional Local Support, the Loaded Cell QC Box was designed at CERN to reduce the influence of varying setups between different production sites within the Outer Barrel community. The design was conceived with the goal that Module Assemblies and Loaded Cells can be tested in the same setup, while by design having varying requirements for the cooling jig. A picture of the box can be seen in Fig. 4.1.

Figure 4.1: The Loaded Cell QC Box setup in Bonn.



(a) (b)

Figure 4.2: Concept drawing of the Loaded Cell QC Box with (a) and without lid (b) [22].

The basic requirements for the Loaded Cell QC Box, derived from the Module QC setup requirements, are:

- Allow safe and efficient cooling of the sensors and readout ASICs in different stages of production down to $-15\,^{\circ}\mathrm{C}$ during operation, which requires a jig temperature of $-45\,^{\circ}\mathrm{C}$.
- Control and monitoring of the environmental conditions in the box.
- Powering of the ITk Pixel module and an interlock solution for the power supplies.
- Simultaneous testing of the functionality of multiple ITk Pixel modules.

A Computer-Aided Design (CAD) drawing of the Loaded Cell QC Box is shown in Fig. 4.2(a). A large lid covers the whole top of the box and beneath it the work area is situated, which can be seen in a cut open side view of the Loaded Cell QC Box in Fig. 4.3. In the large lid four smaller lids are embedded. These smaller lids are placed over the jig positions, to make quick adjustments to the devices under test, without removing the large lid. Beneath the large lid the measuring area of the box is situated. Here are the four jigs positions, the sensors for the interlock and the power and readout adapters for the ITk Pixel modules. Each jig position can be operated individually and is designed for one ITk Pixel module, but is not situated in a separated environment from the others, as can be seen in Fig. 4.2(b). Meaning, when opening a small lid, all test positions need to be shut down.

In the service area for cooling and electronics, most of the cables and tubes for the operation of the jig positions are located. It can be found in Fig. 4.4 and is explained in detail in Section 4.1. The service area for vacuum and dry air supply is the only fully physically separated area of the box and therefore does not need any environmental control. It hosts the switches and external connections for the dry air and vacuum, as well as the switches for the electro valves, that control the water supply for the jigs.

4.1 Mechanical design of the Loaded Cell QC Box

The Loaded Cell QC Box is a $84 \times 79 \times 21\,\mathrm{cm}^3$ (width $\times$ length $\times$ height) large box made of black PMMA, also known as acrylic glass, which is light tight and easy to work with. The service area for

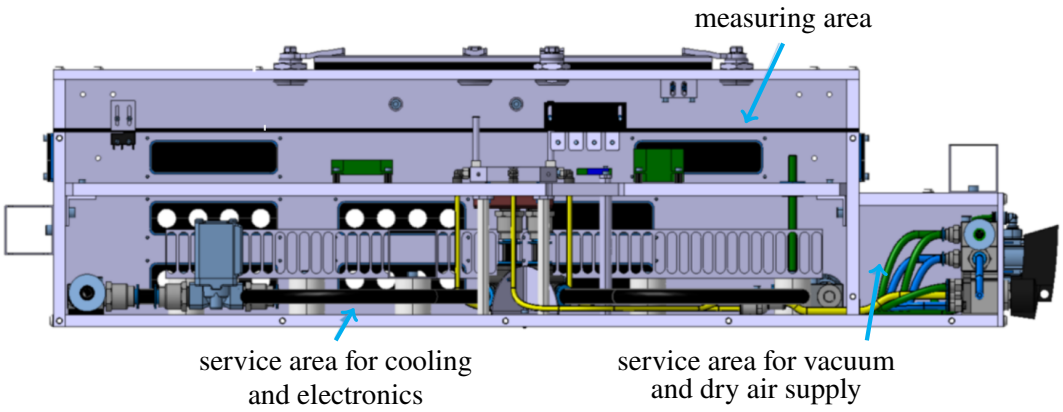


Figure 4.3: Cut open side view of the Loaded Cell QC Box with the three different areas, namely the measuring area, service area and service area for vacuum and dry air [22].

the cooling, vacuum and dry air is $84 \times 67 \times 10\,\mathrm{cm}^3$. A fully populated CAD drawing can be seen in Fig. 4.4. A lot of space is left unused in order to allow for flexibility for possible changes in the future due to updated requirements or differences between the testing sites. To keep the box manageable, the routing of all cables is done in cable ducts. Also, all vacuum, water and dry air pipes are secured to the bottom of the box.

4.1.1 Cooling concept

The ITk Pixel module in its different stages and configurations can be placed on the aluminum cooling block, which is designed for

- bare Module Assemblies,
- Module Assemblies stored in the module carriers,
- Loaded Module Cells,
- Loaded Module Cells stored in the module carriers,

and has been designed to accommodate new devices if necessary. For example, to test the Loaded Cell, four pins of the Bare Cell need to be considered, which can be seen in Fig. 4.5, where four holes are drilled into the aluminum for this purpose.

To reach the specifications of cooling the sensor and readout ASICs down to $-15\,^{\circ}\mathrm{C}$, a temperature gradient between the aluminum cooling jig and the ITk Pixel module of about $30\,^{\circ}\mathrm{C}$ is possible, depending on the stage and setup of the ITk Pixel module. To get down to such low temperatures, two Peltier modules are installed in series beneath the aluminum cooling jig as can be seen in Fig. 4.6. The upper Peltier module has a maximum cooling power of 126.2 W [27] and the lower one of 236.5 W [28]. The in total eight Peltier modules are powered through two HMP4040[1] power supplies, which can source a maximum power of 160 W per channel. This is equivalent to a maximum temperature difference of

[1] Link to the HMP4040 datasheet https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/dl_common_library/dl_brochures_and_datasheets/pdf_1/HMP_dat_en_5215-4981-32_v0201.pdf

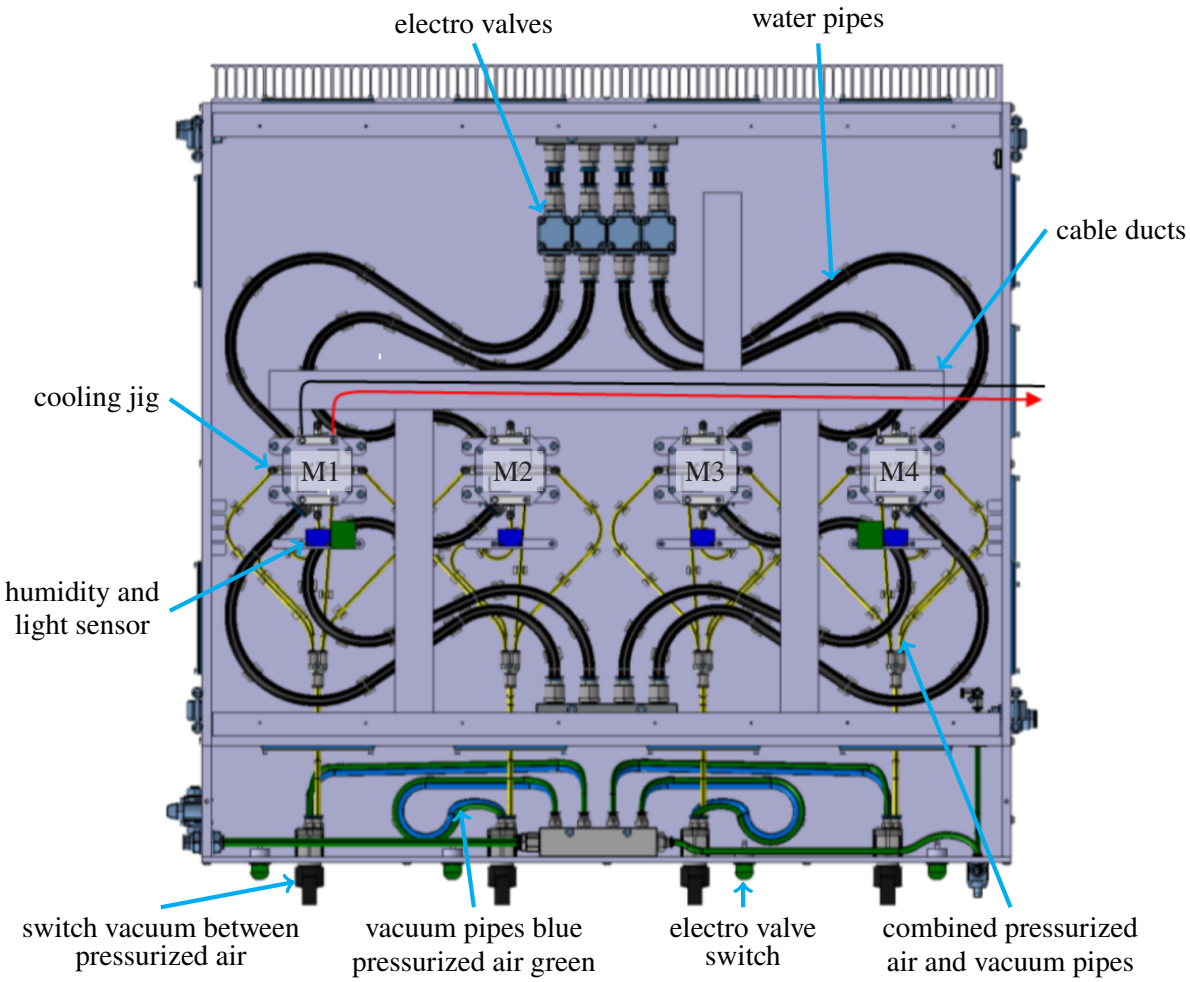


Figure 4.4: Cut open top view of the Loaded Cell QC Box [22]. The four different jig positions and their naming scheme can be seen as well as the adjacent humidity and light sensors. Also the cabling and pipes to run the jigs is shown with the different purposes of the pipes and the control panel on the front.

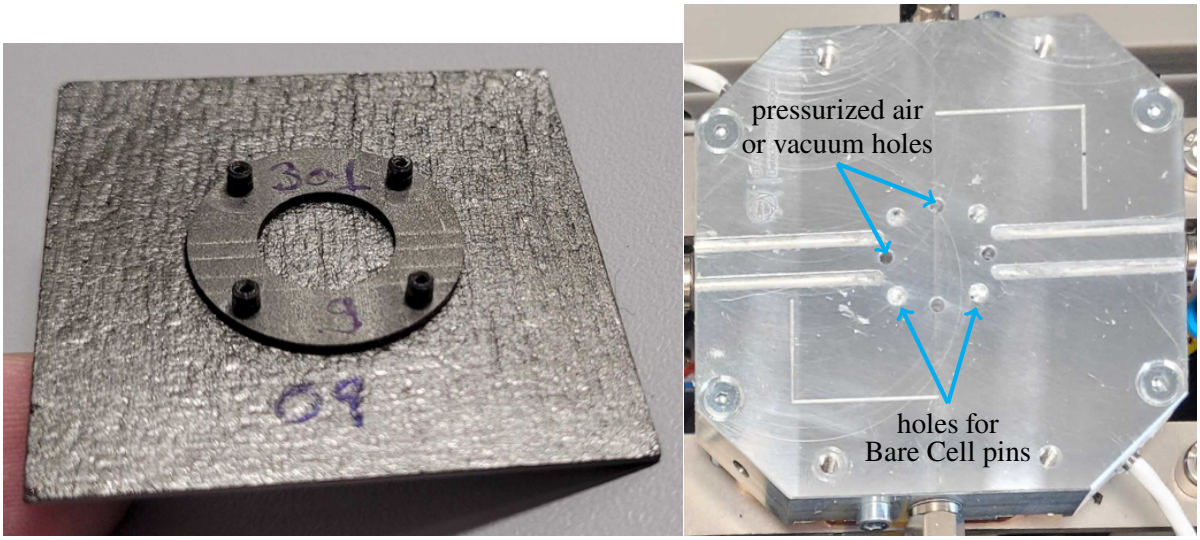


Figure 4.5: Bare Cell (left) and aluminum cooling jig of the Loaded Cell QC Box (right).

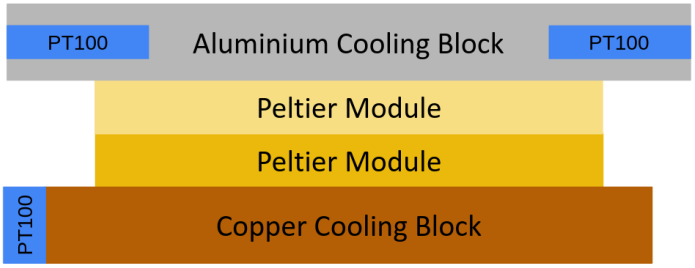


Figure 4.6: Concept for the built-up of the cooling jigs with PT100 temperature sensors.

45 °C for the lower Peltier module and more than 60 °C for the upper one at 20 W heat removal, which is double the amount of power an ITk Pixel module produces, to account for an environmental temperature of 20 °C. As the Peltier modules only create temperature differences, a water cooled copper cooling block is installed beneath the Peltier modules. All four jigs are cooled with the Julabo FP50[2] chiller, which can cool approximately 900 W at 20 °C. The water is guided through the black pipes in Fig. 4.4 and the flow to the different jig positions can be interrupted by the electro valves.

To use all Peltier modules at the same time and to the maximum power, more power supplies and a stronger chiller would be needed, but even with the available cooling power of 225 W per jig it is enough to cool most configurations of the ITk Pixel module on four jigs in parallel. Still, if more cooling power is needed to cool the ITk Pixel module to a sufficient degree, the water flow of the chiller can be directed to just one cooling jig, by closing the water flow to the others and a further power supply can be added to use the full power range of the lower Peltier modules.

[2] Link to the Julabo FP50 datasheet https://assets.fishersci.com/TFS-Assets/CCG/EU/Julabo/Datasheets/Julabo_fp50-me_deutsch.pdf

4.1.2 Dry air and vacuum system

In order to allow for testing over the full required temperature range of the ITk Pixel module, the humidity in the Loaded Cell QC Box must be regulated via a dry air system. A typical requirement throughout the ITk Pixel production is to guarantee a dew point at least 10 °C below the minimum temperature in the respective setup. To reach such low dew points, either a pressurized dry air or a N_2 system can be connected to the box to flush it. In the Forschungs- und Techologiezentrum Detektorphysik (FTD) in Bonn[3], pressurized air with a dew point of −20 °C is accessible in all labs, therefore making it usable for room temperature measurements, where the cooling jigs often only need to be at −10 °C to 0 °C. A dew point measurement for this can be seen in Fig. 4.7.

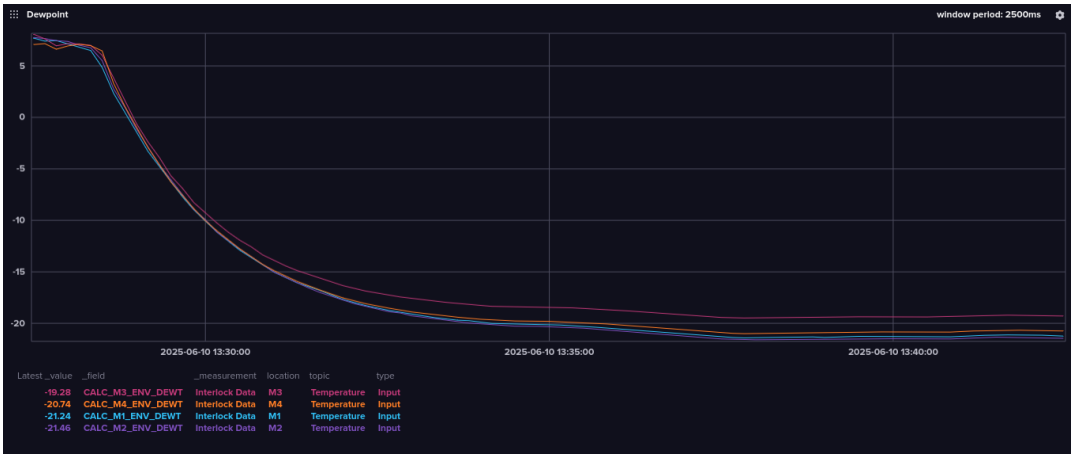


Figure 4.7: The dew point in the Loaded Cell QC Box at the four jigs flushed with pressurized air.

The N_2 system in Bonn can reach a dew point of −60 °C, but is only supplied by large N_2-packs, which are connected to the whole building and therefore need to be refilled weekly. These packs are rather expensive and the usage is limited to the absolute necessary time of operation. For this reason usually pressurized air is used to dry the Loaded Cell QC Box.

The actual measured dew point in the box flushed with the maximum N_2 flow can be seen in Fig. 4.8, where it can be observed that the measured dew point is only −37 °C for one dew point sensor, while another goes down to −55 °C. The reason for this difference between the sensors comes from the accuracy of the used dew point sensors, which is explained more thoroughly in Section 4.2.1. To ensure the safety of the ITk Pixel module the worst dew point is used to trigger the interlock. Therefore in case an ITk Pixel module needs a jig temperature below −10 °C or itself is run at lower temperatures it can be switched to N_2, but the accuracy of the dew point sensors needs to be taken into account, when going to lower temperatures than −27 °C. The dry air system in the box can be identified by the green pipe in Fig. 4.4, which is connected to the pressurized air system of the box in this configuration, as this is the usually used source of dry air in the setup in Bonn.

In the box a combined vacuum and pressurized air system exists, which is connected to four holes in the aluminum jigs, which can be seen in Fig. 4.5. The vacuum system has the purpose to suck the ITk Pixel modules to the aluminum jig and create a tight connection between the ITk Pixel module and the jig to ensure a good thermal connection during testing. The pressurized air is connected to the same holes

[3] Website of the FTD https://www.ftd.uni-bonn.de/de/startseite

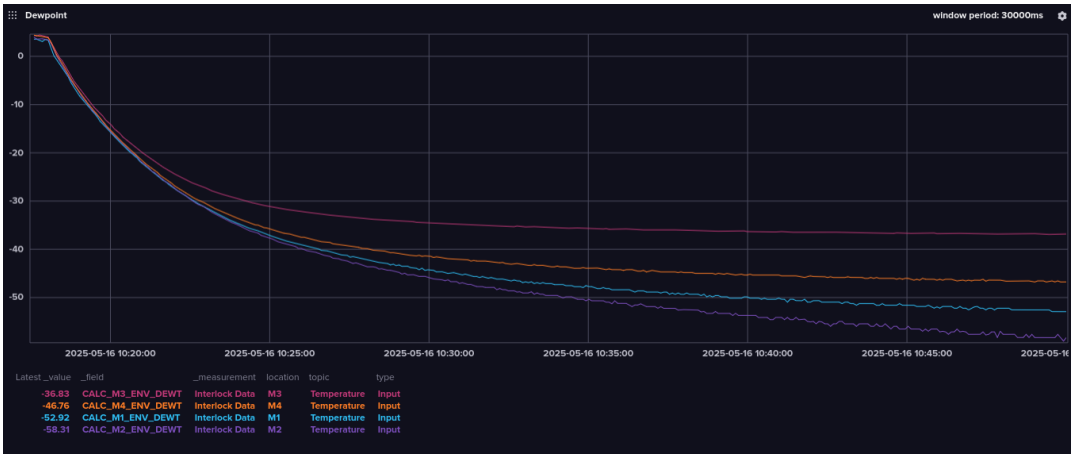


Figure 4.8: The dew point in the Loaded Cell QC Box at the four jigs flushed with N_2.

to clean the pipes and holes in case thermal compound was used for an even better thermal connection. The vacuum system can be identified by the blue pipes and the pressurized air by the green pipes, while the combination of both pressurized air and vacuum pipes to the combined system is depicted with the yellow pipes. The combination of the single systems to the combined system happens at the three way switch, where it can be switched between the pressurized air and vacuum as well as no output.

4.1.3 Improvements to the Loaded Cell QC Box

With the box being designed as versatile as possible for the different sites, a few improvements for the specific use in Bonn have been implemented without compromising the comparability to other sites.

Dry air

As described in Section 4.1.2 the dry air system can be connected to the pressurized air system or the N_2 system in the FTD, both with their respective up and down sides. Therefore it became necessary to switch fast between the two systems during testing. In the standard configuration of the box the process of switching between the two is difficult, because the input pipes to the dry air system need to be switched manually. The connection point for this is inside the service area for vacuum and dry air supply, which is fully enclosed and screwed.

To resolve this problem a switch is installed, which can be seen in Fig. 4.9. To use N_2, the rotary valve must be closed, while the dry air valve needs to be opened. The other way round, pressurized air can be used to flush the box.

Source scans

Originally, source scans were not foreseen to be conducted in the Loaded Cell QC Box, therefore no support structures were built for such a measurement. Nevertheless, for different measurements done in this thesis it became necessary to perform source scans and therefore the setup in Bonn needed to be modified. To perform source scans a few general requirements need to be fulfilled, like a shielding material around the source, a support structure to securely position the source and a placement of the

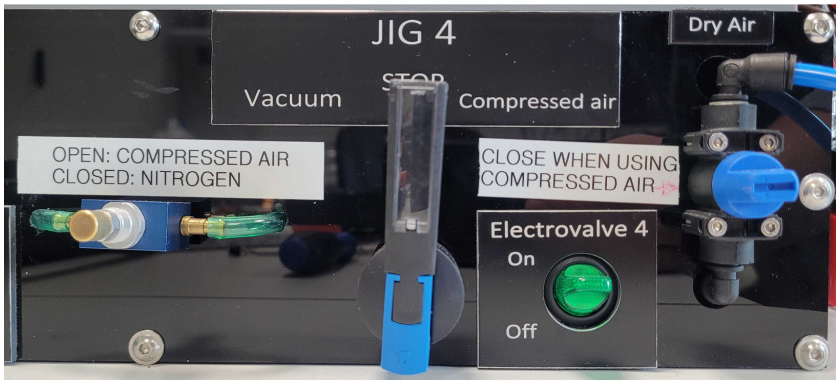


Figure 4.9: Switches between compressed air and N_2.

source close enough to the device under test for a good illumination. The material of the Loaded Cell

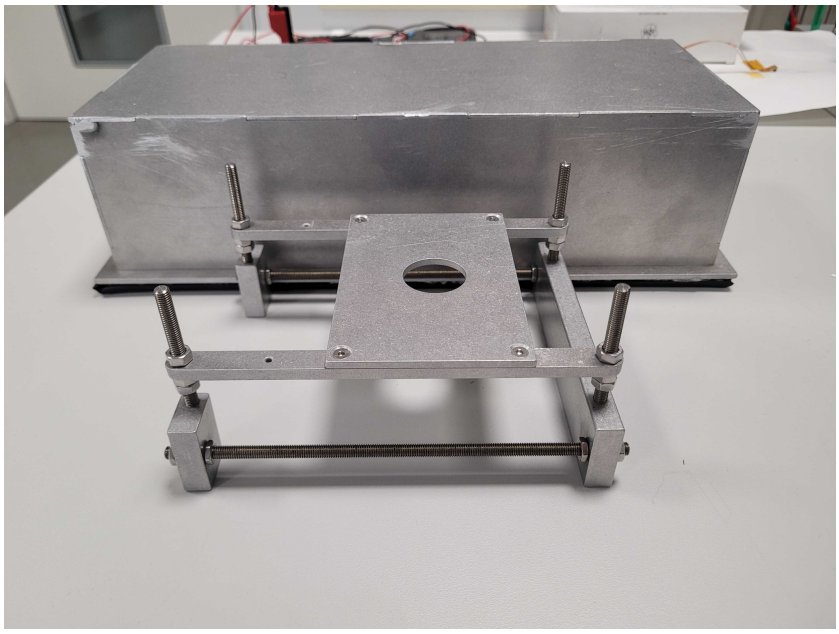


Figure 4.10: Support structure in the foreground and lid out of aluminum in the background for measurements with a source.

QC Box provides enough shielding for a weak gamma source to be placed in it, but the small lid on top leaves not enough space for a support structure and a source. To address this issue an aluminum lid was design to replace one of the four smaller lids, which can be seen in Fig. 4.10.

The support structure, also visible in Fig. 4.10, is designed to allow for flexible positioning of the radioactive sources on top of the ITk Pixel module to ensure a maximum illumination of the active area. It is also designed to not interfere with the electronics and the cabling in the box.

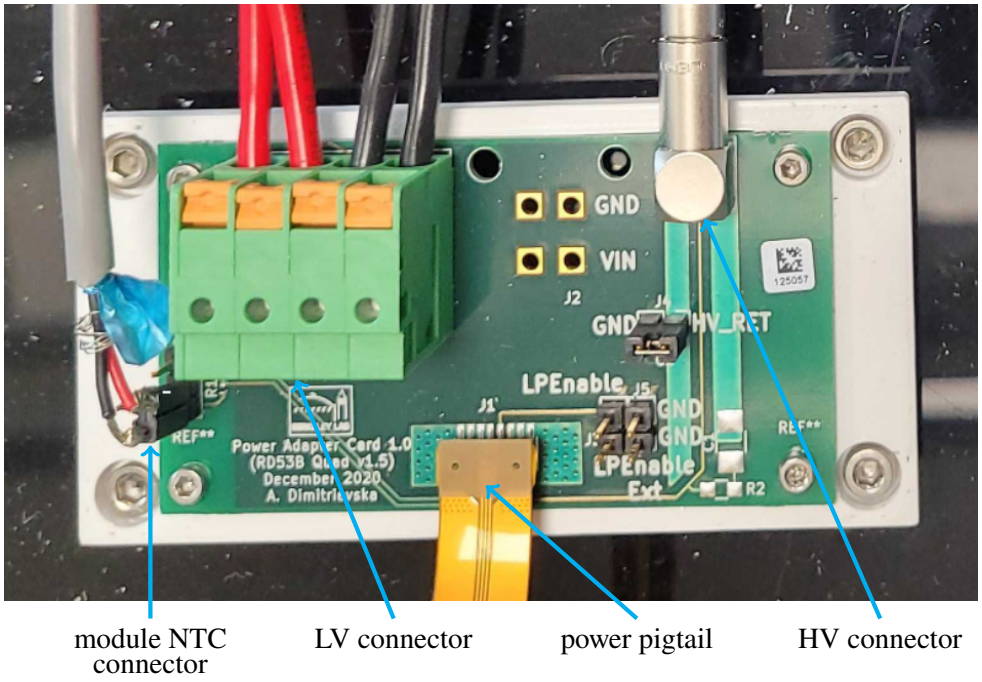


Figure 4.11: The power adapter board, with the connectors for the LV, HV and an NTC readout routed to the power pigtail connector.

4.2 Electrical and control components

The electrical system of the Loaded Cell QC Box consists of three main parts

- the powering of the ITk Pixel modules,
- the readout system,
- and the interlock and its sensor infrastructure.

All of these electronics are routed through cable ducts to keep the box clean and workable. In general, the cabling for power and readout of the modules is done in the working area, while the cabling of sensors and the interlock is routed through the service area for cooling and electronics.

The powering of the ITk Pixel module is achieved through a power adapter card shown in Fig. 4.11, which has connectors for the Low Voltage (LV), High Voltage (HV) and the power pigtail coming from the ITk Pixel module. It also has a connection to readout the module NTC (Negative Temperature Coefficient).

The HV is supplied through a Keithley 2612b[4] with up to 200 V and supplies a current of about 20–60 μA depending on the leakage current of the ITk Pixel module. The LV is supplied via one HMP4040[5] and acts as a current source. The ITk Pixel module requires about 5.88 A with a common

[4] Link to the Keithley 2612b datasheet https://download.tek.com/manual/SPEC-2612B_B_Feb_2014.pdf

[5] Link to the HMP4040 datasheet https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/dl_common_library/dl_brochures_and_datasheets/pdf_1/HMP_dat_en_5215-4981-32_v0201.pdf

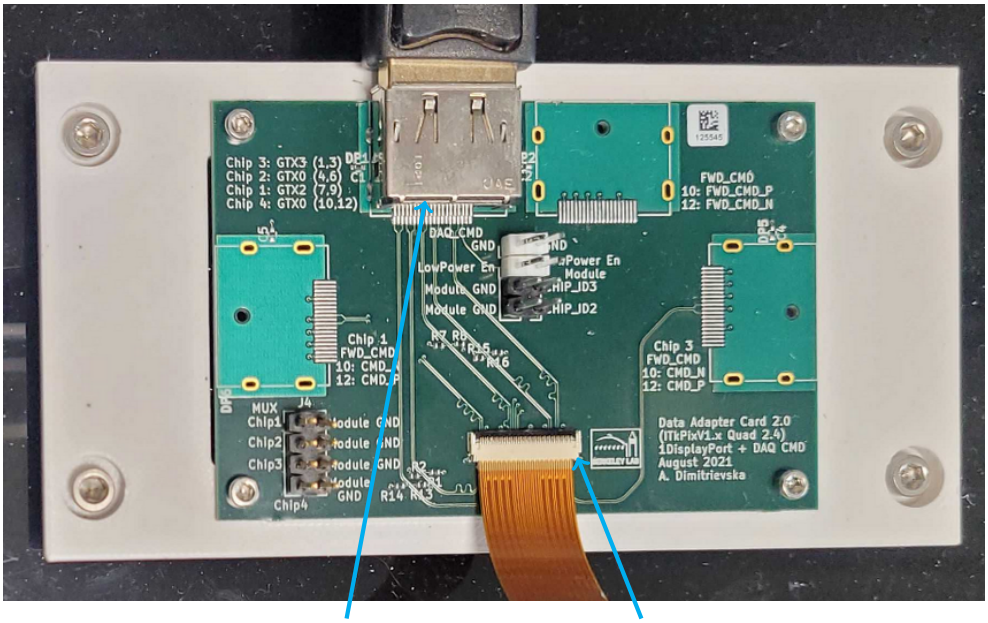


Figure 4.12: The data adapter board, with a Display Port connector routed to the data pigtail connector.

voltage drop over the ITk Pixel modules of about 1.55–1.75 V. In addition to this a voltage drop of about 0.4–0.6 V over the cables, from the power supply to the power adapter card and the power adapter card itself. This adds up to a total power consumption of about 10 W per ITk Pixel module.

The read out of the ITk Pixel module is done via a data adapter board shown in Fig. 4.12, that is connected to the ITk Pixel module through the data pigtail. The data adapter board can then be connected to a readout system via a Display Port cable, in the case of Bonn the BDAQ board. The BDAQ board can read out one ITk Pixel module at a time and transmit the data to the computer to analyze it. For a faster testing cycle it would be possible to connect four BDAQ boards to a computer and read out all jig positions at the same time, but for the time being the Loaded Cell QC Box is setup with one BDAQ board.

4.2.1 Interlock system

The principle of any interlock is to utilize sensors to identify threats to the DUT and trigger an action if the sensors pass certain thresholds to avoid damage to the DUT. To achieve this, there are mainly three different types of systems deployed, a hardware, software and firmware interlock. As a general rule, software interlocks are considered to be inferior to hardware interlocks and a good middle ground between the two is the firmware interlock. While a hardware interlock only relies on fuses or similar equipment, a software interlock reads data and a computer program activates switches or turns off devices via a command transmission. While a hardware interlock is much less vulnerable to programming and connection errors or the processor running it failing, a software interlock is a lot more flexible without the change of hardware components. A firmware interlock on the other hand is a combination of the two concepts, where a separate processor, usually a micro controller, reads out the data and sends a signal to

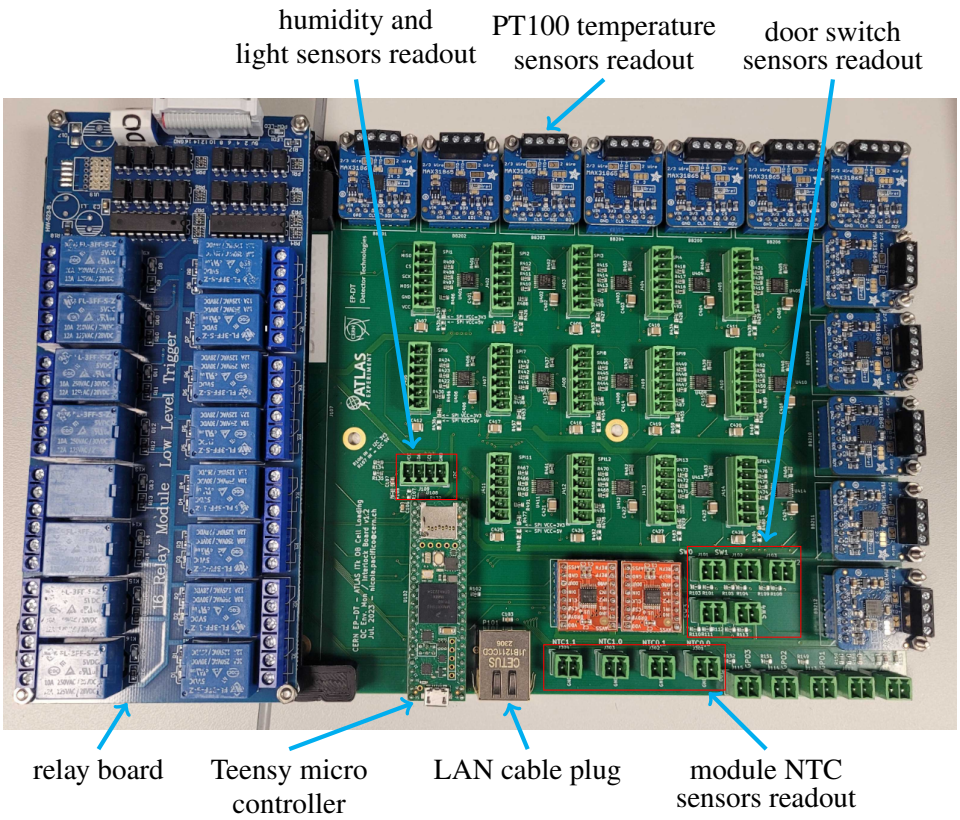


Figure 4.13: The interlock board for the Loaded Cell QC Box with the different connection points to the sensors, the Tennsy micro controller and the relay board.

the hardware. The difference to a software interlock is, that the micro controller is mounted together with the hardware interlock components it controls on a singular PCB. This method is similarly susceptible to errors in the program as a software interlock, but a crash of the system is very unlikely, as the only purpose of this micro controller is to handle the interlock.

For these reasons, a firmware interlock is implemented to the Loaded Cell QC Box with a PCB designed at CERN, which is shown in Fig. 4.13.

The processing on the board is done by a Teensy[6] micro controller run with a firmware programmed at CERN [29], which controls a relay board with sixteen relays. These relays are planned to control the power supplies for the LV, HV and the Peltier modules by sending a digital interlock signal. However, the used power supplies (HMP4040 and Keithley 2612b) do not have integrated interlocks and therefore cannot be controlled by a digital interlock signal. To solve this, the digital interlock signal from one relay is sent to two other relays. These relays act as switches in between the power and ground cables going from the power supply to the components. With this setup, each controlled channel needs two relays, which adds up to 32 relays in total from the four LV, four HV channels and the eight Peltier modules, each supplied by one channel of the power supply.

To decide when to set an interlock, the micro controller reads out four different types of sensors,

[6] Link to the Teensy micro controller https://www.pjrc.com/store/teensy41.html

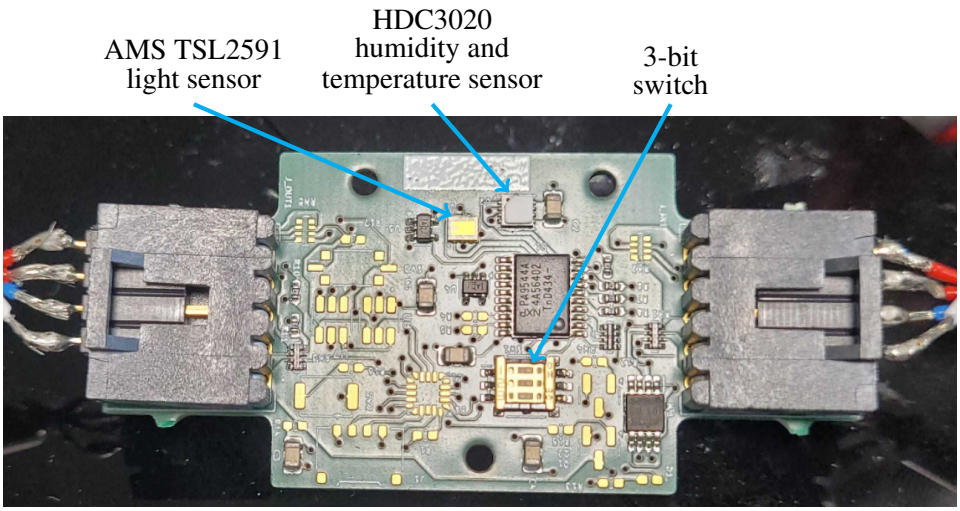


Figure 4.14: Light and humidity sensor board in the Loaded Cell QC Box, with the two sensors and a 3-bit switch.

namely door switches, dew point sensors, light level sensors and temperature sensors. In total 31 sensors are connected to the interlock board. The connection points on the interlock board can be seen in Fig. 4.13.

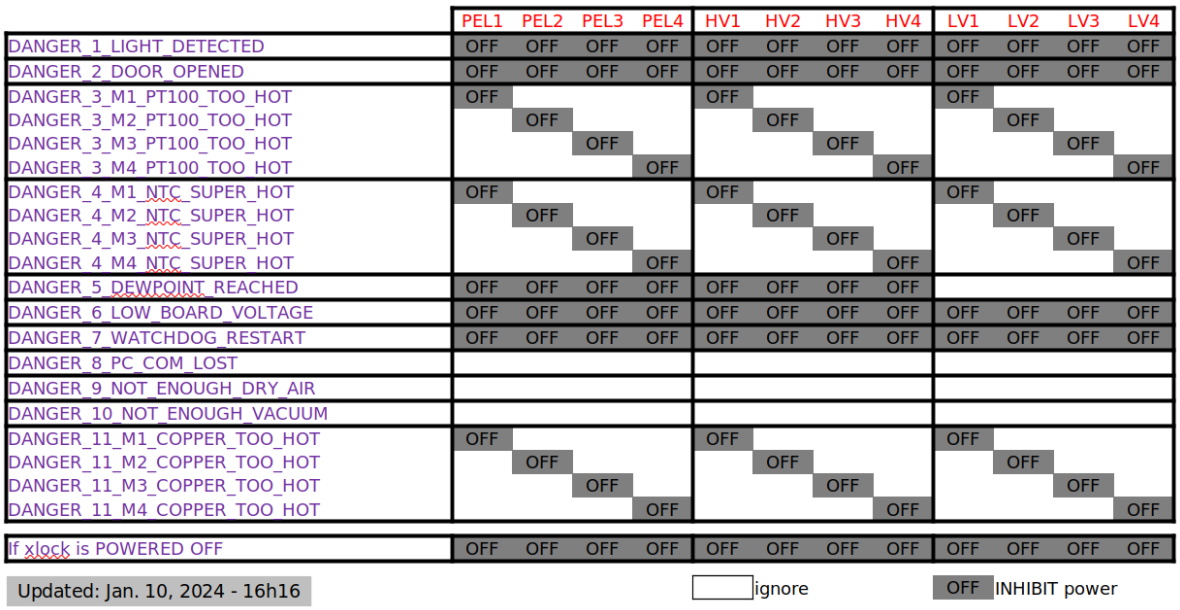
Each door in the box is monitored by a simple switch and with four small lids and one large lid the interlock has five available sensor inputs to monitor the doors. The dew point and the light level is measured at four different spots in the box close to the jig positions, which can be seen in Fig. 4.4. The sensor for the dew point in use is a HDC3020[7]. This sensor is rather cheap and has an accuracy of 1% relative humidity below a measured relative humidity of 5%. This accuracy error can lead to a difference in the dew point of up to 20 °C beneath the 5% relative humidity threshold. For the light level a AMS TSL2591[8] is used. Both sensors are mounted on the same PCB, which can be seen in Fig. 4.14. These boards are daisy chained, which makes the three bit switch on the PCB necessary, as each address determines a position of the sensor in the setup. For example *000* corresponds to jig position M1.

To measure the temperature of the jigs multiple PT100 temperature sensors are installed, which can be seen in Fig. 4.6 and add up to in total 12 sensors for all jigs, each read out by a special readout board on the interlock board. Because these sensors only measure the jig temperature, also the NTC temperature of the ITk Pixel module is read out through a connection on the power adapter card as can be seen in Fig. 4.11 and as four ITk Pixel modules can be tested at once, also four spots for the NTC readouts are available on the interlock board.

All of these measurements get processed by the interlock board, which following the logic table in Fig. 4.15 then cuts off the power supplies. For example, opening any door, will result in the danger *DANGER_2_DOOR_OPENED* detected and a shut down of all power supplies, while a too high temperature on jig one, will result in *DANGER_3_M1_PT100_TOO_HOT* detected and a power cut to the HV, LV and Peltier modules for jig one (in this case).

[7] Link to the HDC3020 datasheet https://www.ti.com/lit/ds/symlink/hdc3020.pdf?ts=1750350596346&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252Fde-de%252FHDC3020

[8] Link to the AMS TSL2591 datasheet https://docs.rs-online.com/df3d/0900766b814cdbc5.pdf



	PEL1	PEL2	PEL3	PEL4	HV1	HV2	HV3	HV4	LV1	LV2	LV3	LV4
DANGER_1_LIGHT_DETECTED	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DANGER_2_DOOR_OPENED	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DANGER_3_M1_PT100_TOO_HOT	OFF				OFF				OFF			
DANGER_3_M2_PT100_TOO_HOT		OFF				OFF				OFF		
DANGER_3_M3_PT100_TOO_HOT			OFF				OFF				OFF	
DANGER_3_M4_PT100_TOO_HOT				OFF				OFF				OFF
DANGER_4_M1_NTC_SUPER_HOT	OFF				OFF				OFF			
DANGER_4_M2_NTC_SUPER_HOT		OFF				OFF				OFF		
DANGER_4_M3_NTC_SUPER_HOT			OFF				OFF				OFF	
DANGER_4_M4_NTC_SUPER_HOT				OFF				OFF				OFF
DANGER_5_DEWPOINT_REACHED	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF				
DANGER_6_LOW_BOARD_VOLTAGE	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DANGER_7_WATCHDOG_RESTART	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DANGER_8_PC_COM_LOST												
DANGER_9_NOT_ENOUGH_DRY_AIR												
DANGER_10_NOT_ENOUGH_VACUUM												
DANGER_11_M1_COPPER_TOO_HOT	OFF				OFF				OFF			
DANGER_11_M2_COPPER_TOO_HOT		OFF				OFF				OFF		
DANGER_11_M3_COPPER_TOO_HOT			OFF				OFF				OFF	
DANGER_11_M4_COPPER_TOO_HOT				OFF				OFF				OFF
If xlock is POWERED OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Figure 4.15: The interlock logic table[9] with the different dangers and which kind of power supply they shut down. Here PELx are the power supplies for the Peltier modules, HVx are the once for the HV power supplies and LVx are the power supplies for the LV.

To monitor the activities of the interlock system, a connection to a local PC can be set up. Here, the data monitored and sent out by the Teensy can be processed by a graphic user interface (GUI) [30], which displays the data as shown in Fig. 4.16. On the left one can see the values measured in the box, with the dew point being calculated from the ambient measures. The *Dangers* column shows the immediate threats for the modules, with the intervals for the different quantities considered to be safe being defined as [31]:

- PT100 temperature sensor of aluminum cooling block at maximum 30 °C.
- PT100 temperature sensor of copper cooling block at maximum 40 °C.
- NTC temperature of the ITk Pixel module at maximum 40 °C.
- Light level of maximum 10% of the sensors range.
- Dew point at least 10 °C lower than any temperature sensor.

If a value of a monitored quantity is out of the interval that is considered safe, an interlock is set for this value. These interlock signals are then translated to the *Controlled devices* column, where it is shown which power supplies are cut off. The set interlocks can only be manually set back by an operator with the button *RESET LOCKED-IN INTERLOCKS*.

In case further analysis is needed, the measured values and interlock signals are stored in an influx database on the PC. These values then can be converted to graphs or block diagrams, to be more easily

[9] Link to the interlock logic table https://box.in2p3.fr/index.php/s/ykqKfcNtp87tm5F

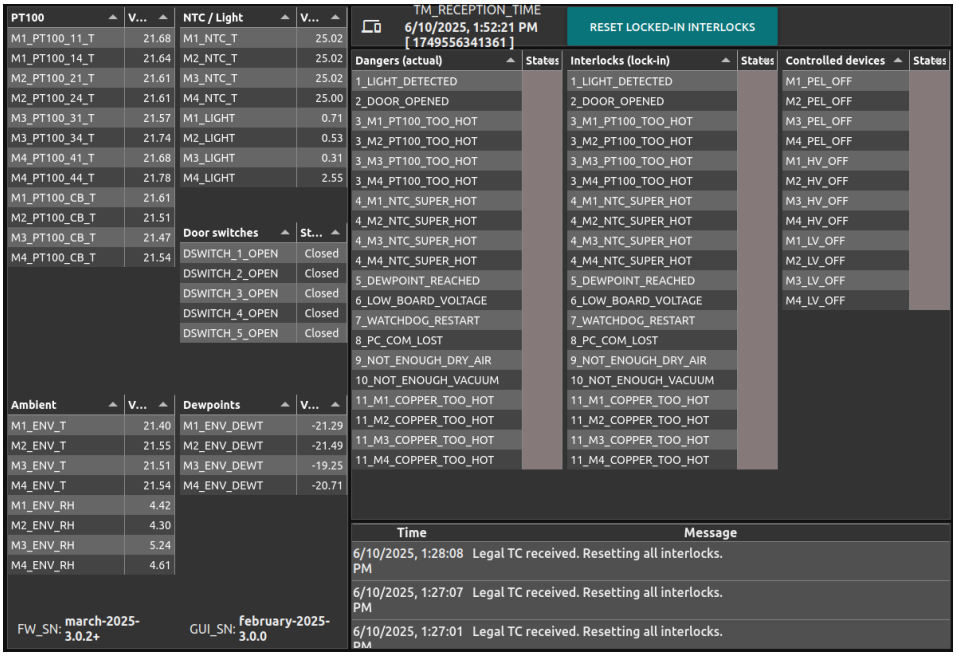


Figure 4.16: The interlock GUI with the different temperature, dew point, light level and door sensors on the left and the dangers and the adjacent interlock responses on the right.

analyzable for a human operator and allow to reconstruct failures that occurred during the absence of the operator. Examples for this can be seen in Fig. 4.17, where different sensor readouts for each jig position are displayed, like the copper block temperature, aluminum block temperature, general box temperature and the light level. These measurements were performed with no device or cooling activated and only the lids closed.

Figure 4.17: Different sensor readouts displayed in the Influxdb like the copper block temperature, aluminum block temperature, general box temperature and the light level. The measurements were conducted with no device or cooling in the box and with the lids closed.

4.3 Validation of the Loaded Cell QC Box with a digital ITk Pixel module

To validate the functions of the Loaded Cell QC Box, a digital ITk Pixel module was delivered with the box. A digital ITk Pixel modules is built only from the readout ASIC and a flex PCB and is missing the sensor. To validate the Loaded Cell QC Box, a digital, analog and threshold scan, also called a Minimum Health Test (MHT), was conducted on all four jig positions with this digital ITk Pixel module. At the time, this test was a standard measure to test the functionality of an ITk Pixel module in the Outer Barrel community and therefore was chosen for this validation. Once available a fully functional ITk Pixel module with a planar sensor was used to validate the Loaded Cell QC Box. To conduct all these scans, the digital ITk Pixel module needs to be running stable at room temperature with the interlock active.

To verify the interlock, several tests were conducted. In these tests, conditions were created, where one sensors registers a value above its interlock threshold and it is checked if the right interlock condition is triggered. An example for this can be seen in Fig. 4.18, where a door switch is opened and the interlock *INTERLOCKED_2_DOOR_OPENED* is set, which deactivates all power supplies. It can also be seen, that the interlock is still locked in after the door is closed again. To unlock it the *RESET LOCKED-IN INTERLOCKS* button in the interlock GUI needs to be pressed.

The first step to run the scans is to place and connect the digital ITk Pixel module on the jig position, that shall be tested. After turning on the cooling, the LV can be switched on and afterwards the digital ITk Pixel module can be stabilized at room temperature with an adjustment of the Peltier modules cooling power. The module NTC temperature during a power up of the digital ITk Pixel module can be

Figure 4.18: An interlock reaction to the opening of a door switch displayed in the influxdb to validate the interlock system.

seen in Fig. 4.19, where first the Peltier modules cool the digital ITk Pixel module to 10 °C and after the power up it goes back up to 20 °C. The digital ITk Pixel module runs with a similar power consumption of 10 W like the standard ITk Pixel module and therefore generates a similar amount of heat and keeping it at room temperature requires a fully functional cooling system.

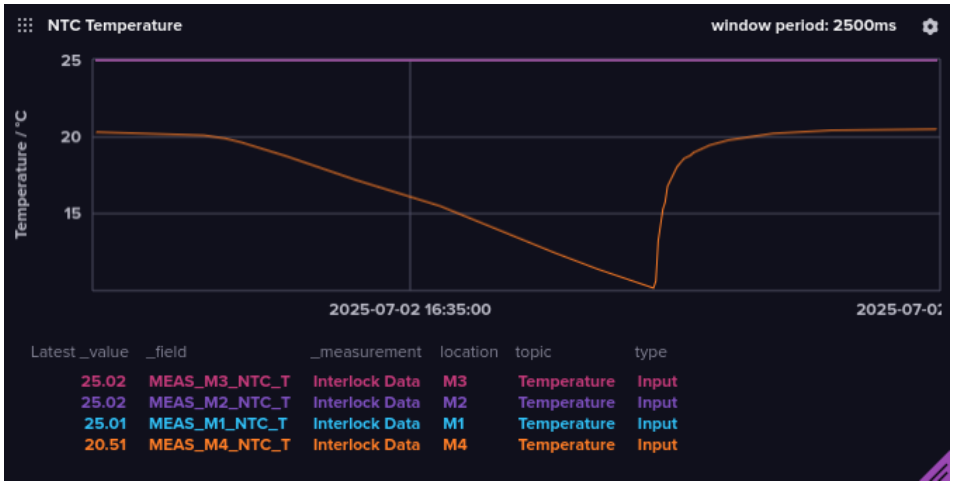


Figure 4.19: An example for the temperature of the digital ITk Pixel modules during a start up.

In this configuration, the digital scans for all four jig positions are shown in Fig. 4.20. The scan results are the same for all jig positions and are working as expected.

The same holds for the analog scan, which can be seen in Fig. 4.21. When comparing the expected Occupancy of $\sum = 61440000$, which one gets by multiplying the 100 injections in the standard BDAQ

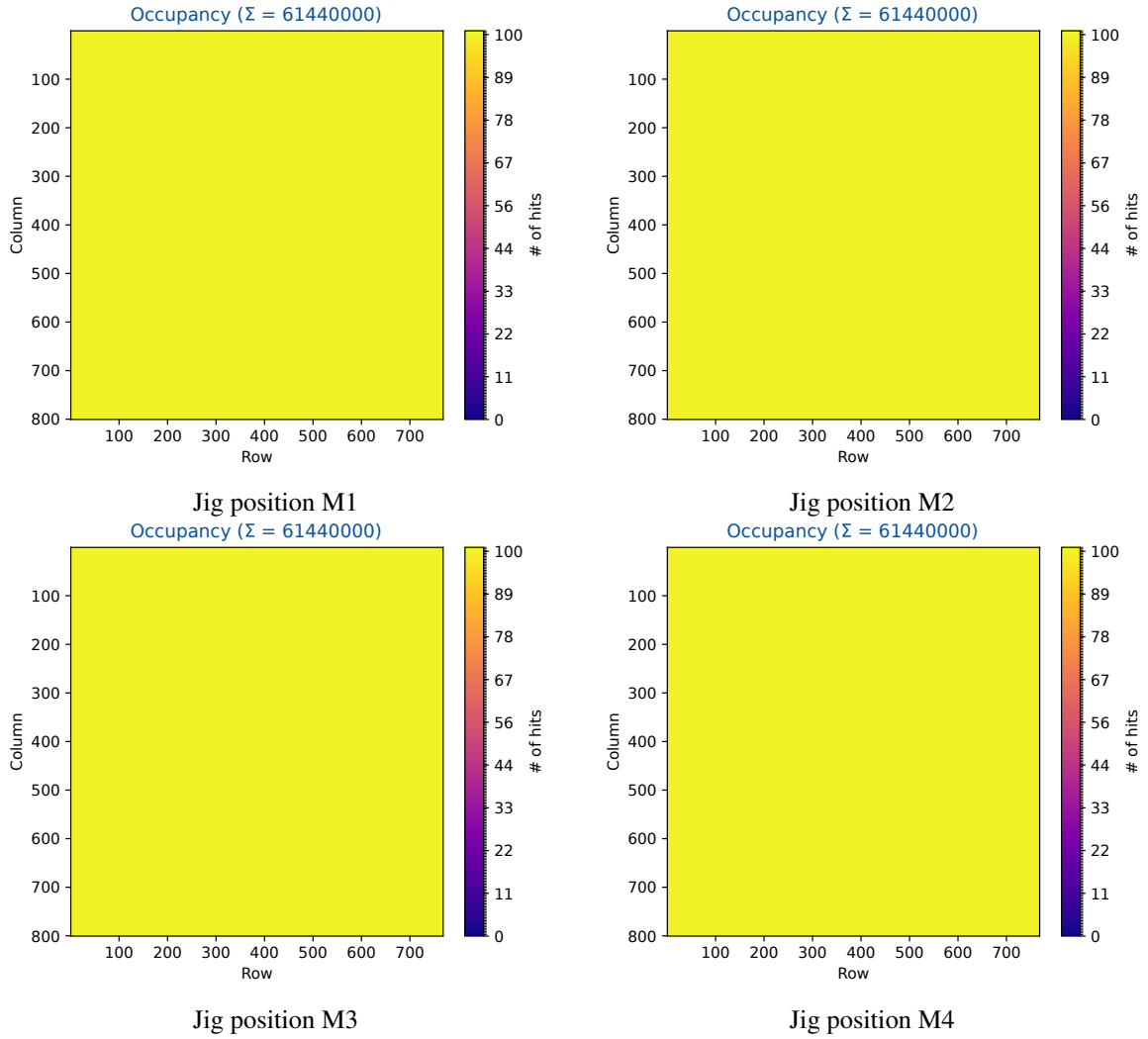


Figure 4.20: Occupancy maps of a digital ITk Pixel module with 100 digital test injections for each jig.

analog scan with the number of pixels on an ITk Pixel module from Section 3.2, to the measured Occupancy of $\sum = 61439900$, precisely 100 hits are missing. Upon closer investigations it became clear that these missing hits all originate from the same pixel with an occupancy of 0.

For the threshold performance analysis, the module was first tuned to 1 000 e^-. As can be seen in Fig. 4.22, a threshold of 1 000 e^- was achieved with a similar standard deviation of about 18 e^- for all jig positions of the digital ITk Pixel module.

To fully validate the Loaded Cell QC Box the only missing test is an IV curve. For this purpose one ITk Pixel module with sensor was used, which only became available after the first validation of the box with the digital ITk Pixel module. The IV curve of the sensor for all four jig positions is measured and displayed in Fig. 4.23. The HV for an unirradiated ITk Pixel module has usually a leakage current of a few 10 nA up to a maximum of 100 μA when used with up to 200 V reverse bias voltage [25].

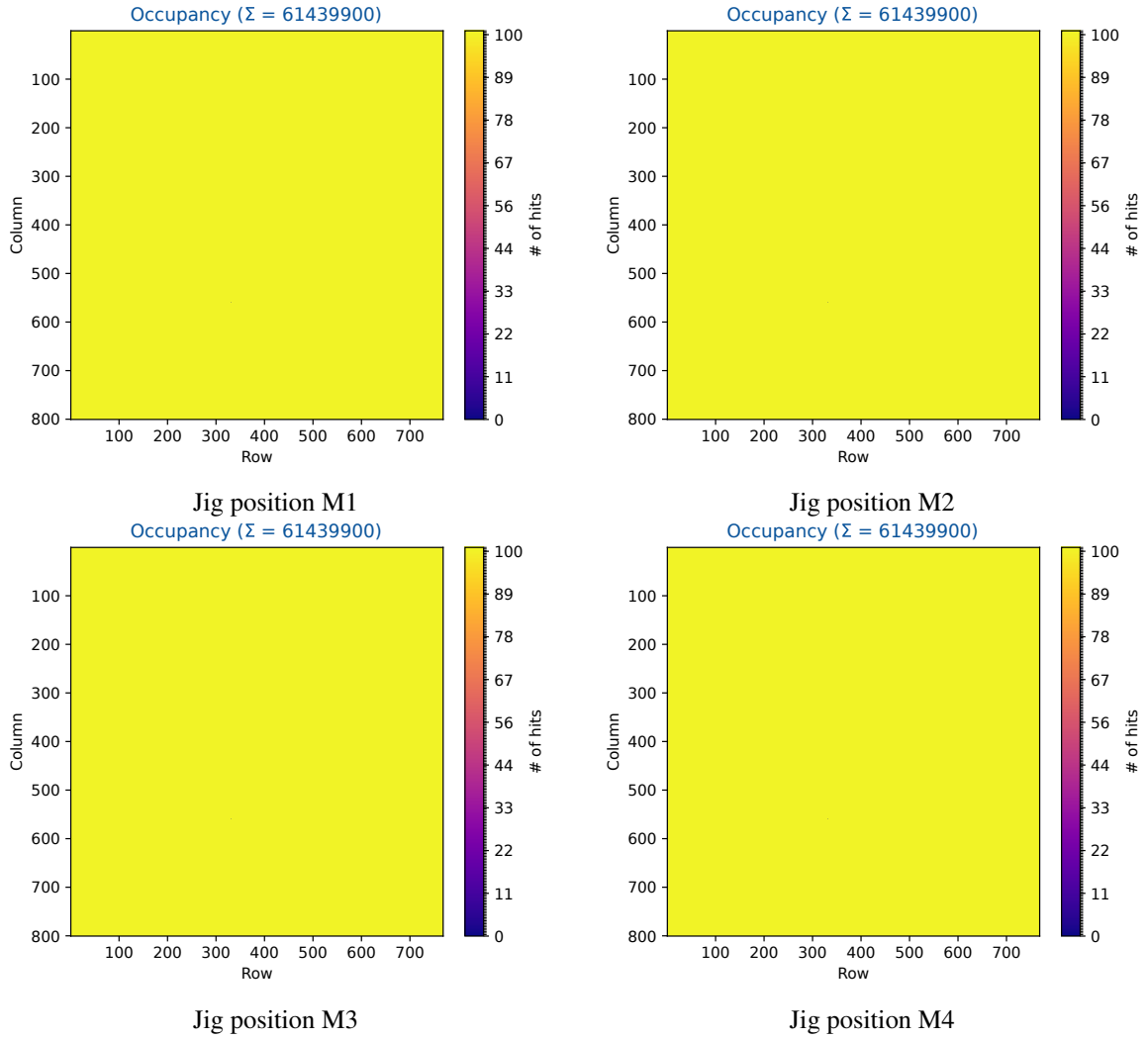


Figure 4.21: Occupancy maps of a digital ITk Pixel module with 100 analog test injections for each jig.

The leakage current of a sensor should have a diode like behavior as explained in Section 2.2.2. The tested ITk Pixel module shows this behavior on each jig, as for a large range of voltages the leakage current only increases slightly. However, the test voltages are not high enough to reach the break down voltage of this ITk Pixel module sensor, which is also not expected in this voltage range. The differences in leakage current for the different jig positions comes from the temperatures of the ITk Pixel module on the jigs.

With all of the tests successfully completed, the Loaded Cell QC Box is qualified for its intended purpose, the Loaded Cell reception of multiple ITk Pixel modules.

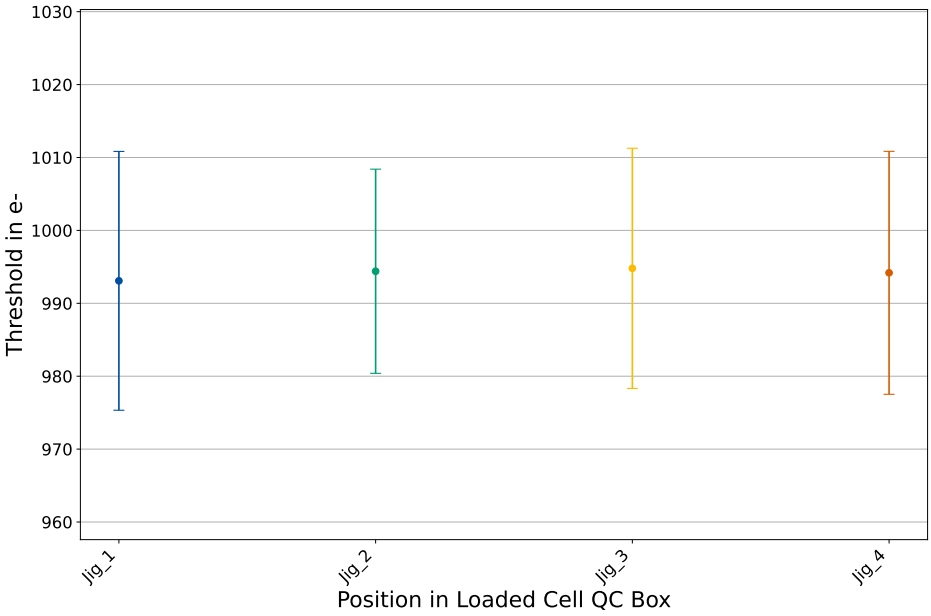


Figure 4.22: Mean threshold for each chip on each jig position of an ITk Pixel digital module after a tuning to 1 000 e^-.

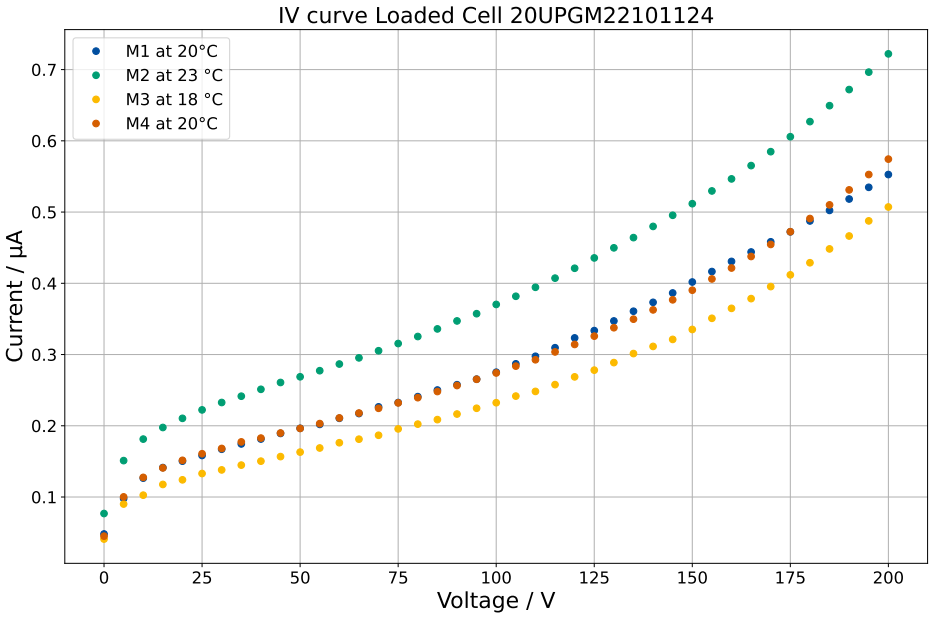


Figure 4.23: The sensor IV curve of an ITk Pixel module with the reverse bias voltage on the x-axis and the measured current on the y-axis.

CHAPTER 5

Source scans on ITk Pixel modules for a bump bond stress test

ITk Pixel modules are hybrid pixel detectors, consisting of a separate sensor tile and readout ASICs, which are bump-bonded in a process called flip chipping. These bump bonds are only the size of a few μm and the large amount of the bump bonds on one ITk Pixel module makes the flip chip process a very expensive and time-consuming endeavor. If the bump bonds break, the pixel cannot detect charge anymore, which lowers the efficiency of the ITk Pixel module over all. Usually only a few bump bonds on an ITk Pixel module are disconnected after production and a threshold of 614 disconnected bumps is considered still acceptable for the ITk Pixel module and the physics requirements of the ITk. A further disconnection of bump bonds after production arises, when they are exposed to mechanical stress. This can happen, when the ITk Pixel modules are picked up, endure mechanical shocks or extensive thermal fluctuations. While the first two mechanical types of stress can be mostly avoided, thermal cycles are an inevitable part of the start up and life of the ITk. Therefore it was decided to test, how thermal cycling influences the bump bonds and if this could become a problem during the runtime of the ITk, which is expected to endure about 100 thermal cycles between operating temperature of $-20\,^{\circ}\mathrm{C}$ and room temperature.

For this purpose eight Loaded Cells were prepared and the goal was to cycle them 1000 times, to see how durable the Loaded Cells are. To do so, a climate chamber at the University of Göttingen was used and after an initial cycling of the eight Loaded Cells at CERN for 100 times, they were sent to Göttingen for the full test run.

In the beginning, the Loaded Cells are tuned to $1\,500\,\mathrm{e}^{-}$ and afterwards the testing procedure can start with a digital and analog scan as explained in Section 3.2.1. This generates a new mask, of pixels that are digital and analog failing and afterwards a cross talk disconnected bump scan is conducted. With these tests completed the Loaded Cells undergo 50 thermal cycles from $-55\,^{\circ}\mathrm{C}$ to $60\,^{\circ}\mathrm{C}$ with a temperature change of $1\,^{\circ}\mathrm{K}$ per second. This procedure, apart from the tuning, is then repeated until the 1000 thermal cycles are reached, or a Loaded Cell shows an increasing number of disconnected bumps.

The information about the procedure combined with the raw data supplied for several plots with data from Göttingen in this Chapter are kindly supplied by J. Grosse-Knetter et al. [32]. The serial number will be abbreviated to maintain readability in this thesis, for example the module 20UPGM2210121 is referred to as module 121.

From this scan routine a disconnected bump count after each 50 cycles can be created. The result

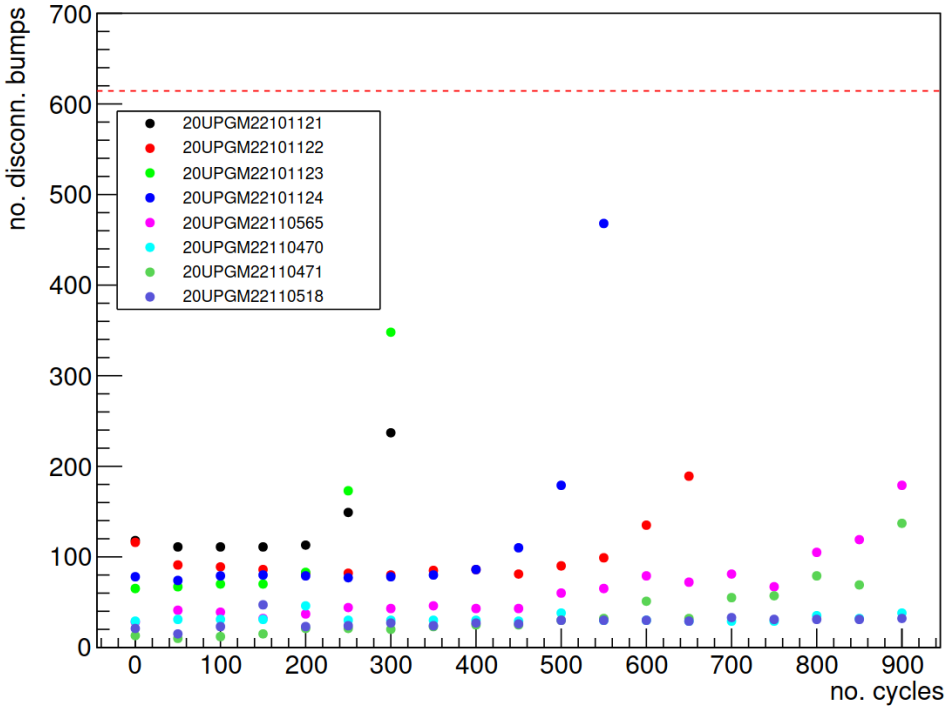


Figure 5.1: Number of disconnected bumps for eight Loaded Cells after going through a number of thermal cycles in Göttingen to test the bump bonds against thermal stress and the maximum threshold of 614 disconnected bumps marked as the dashed red line [32].

of this can be seen in Fig. 5.1. As can be seen the number of disconnected bumps fluctuates between measurements on each Loaded Cell. This is because the mask is renewed before each disconnected bump scan and a fluctuation of about 20 pixels is expected. The first major increase for the Loaded Cells 121 and 123 starts after about 250 and for the Loaded Cells 122 and 124 after about 500 thermal cycles in Göttingen. This relatively early rise of disconnected bumps was not expected and also the position of the areas of delamination were unexpected, which can be seen as an example for the Loaded Cell 121 in Fig. 5.2. The areas of disconnected bumps started forming in the middle of the readout ASICs, which is unusual as the most mechanical stress through thermal cycling would be expected at the edges of the readout ASICs.

Because of these observations, it was suggested to validate the cross talk disconnected bump scan through a radioactive source disconnected bump scan. However, the module test setup in Göttingen could not accommodate Loaded Cells, because the Cooling Block pins and the climate chamber in which they could be cooled alternatively was not certified to use a source inside. However, it was possible to conduct these scans with the Loaded Cell QC Box in Bonn, because it can handle Loaded Cells and was upgraded to perform source scan as described in Section 4.1.3. For this reason, the Loaded Cells 121, 122, 123 and 124 were shipped to Bonn to perform a source scan and compare the observed disconnected bumps with both scan methods.

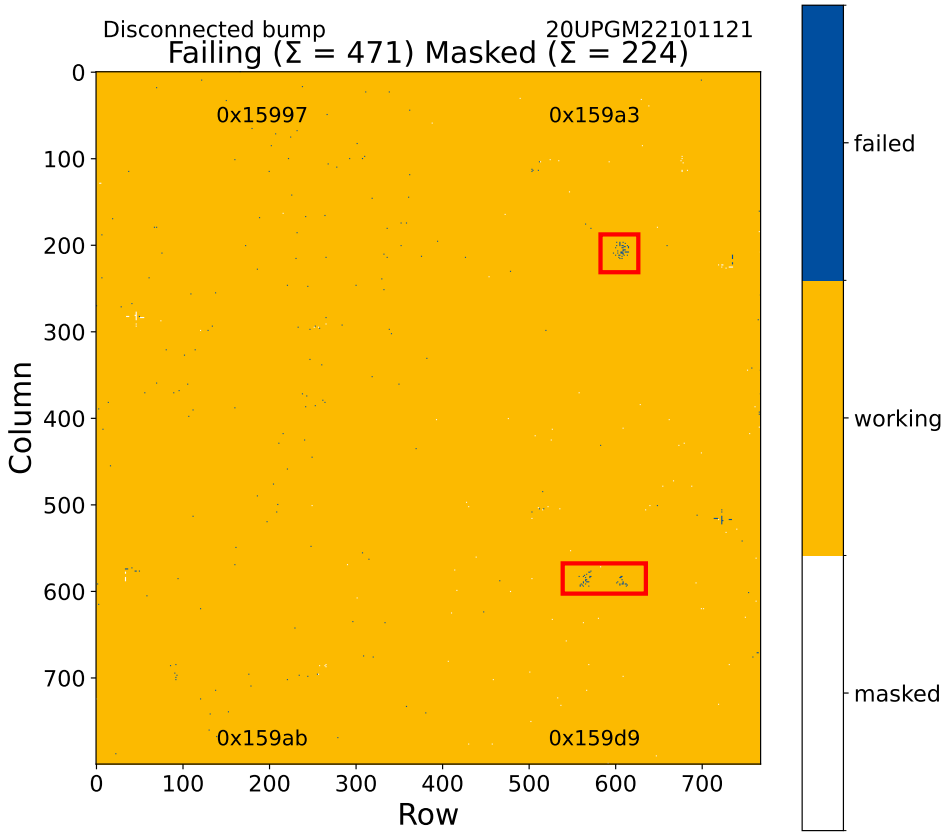


Figure 5.2: Disconnected bump map from a cross talk disconnected bump scan for the whole Loaded Cell 121 with delamination areas in the middle of the readout ASICs visible by the red rectangles.

5.1 Performance test after transport

When the Loaded Cells arrived in Bonn, a MHT was performed to guarantee the functionality and look for damages after transport. For this test each ITk Pixel module came with configurations supplied from Göttingen, which includes a masking, disabling the analog and digital bad pixels with the criteria shown in Section 3.2.1.

The comparison of the digitally failing pixels between Bonn and Göttingen can be found in Fig. 5.3. For this scan the masking from Göttingen was not reset in Bonn and as expected, when no transport damage occurred, the Loaded Cells showed no failing pixels.

The results for the analog scan can be found Fig. 5.4. In this scan, the mask was reset for the Loaded Cells 123 and 124, but not for the other two. This reset of the masks was not intended, but a failure of

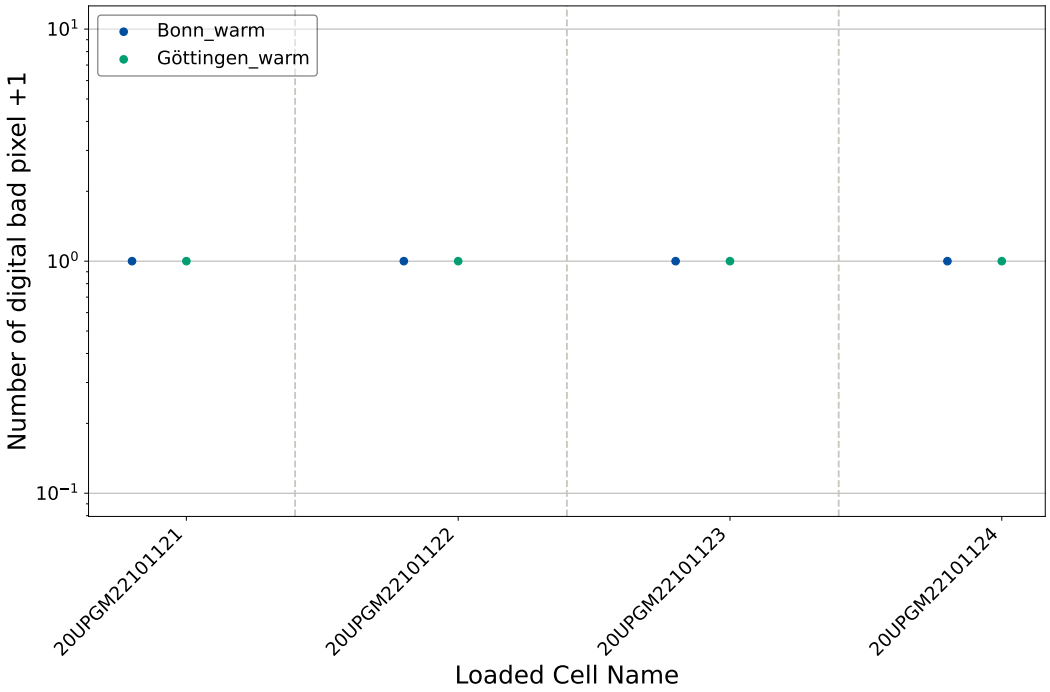


Figure 5.3: Comparison of the digital failing pixels per Loaded Cell between Bonn and Göttingen with the serial number of the Loaded Cell on the x-axis and the number of failing pixels on the y-axis.

the conversion of the configuration from YARR, used in Göttingen, to BDAQ, used in Bonn. For both testing facilities similar numbers of failing analog pixels can be found and the results are comparable.

As no threshold scan was performed in Göttingen, no comparison between the sites is possible, but the Loaded Cells were initially tuned to 1 500 e^-, which can be verified. The results of the threshold scan can be found in Fig. 5.5 and shows a good match for all Loaded Cells to the expected value of 1 500 e^-. The conclusion of the MHT is that the Loaded Cells sent to Bonn do not exhibit any sign of transport damage. Therefore, the planned disconnected bump scan, via a self trigger source scan, can be carried out to compare the two methods, as the Loaded Cells have not degraded from Göttingen to Bonn.

5.2 Results of the disconnected bumps scans

The source used for the self trigger source scan is a ^{241}Am area source, which emits mainly alpha and gamma radiation like $^{241}\text{Am} \rightarrow^{237} \text{Np} + \alpha(5.48\,\text{MeV}) + \gamma(0.014\,\text{MeV})$, from which the alpha radiation is blocked through a window. The ^{241}Am source can be placed on the support structure with the opening over the hole in the source support structure described in Section 4.1.3. To get a good illumination of the ITk Pixel module, the source is placed about 3 cm above the ITk Pixel module. Because ^{241}Am is only a low energy γ-source in this configuration, the photons are easily absorbed by any material on their pass and the scan needs to run about 3.5 hours to get a good illumination on the Loaded Cells.

The resulting source scans can be found in the Fig. 5.6. Here the SMD components on the module flex block some of the radiation and are clearly visible, as well as the position of the source, which is

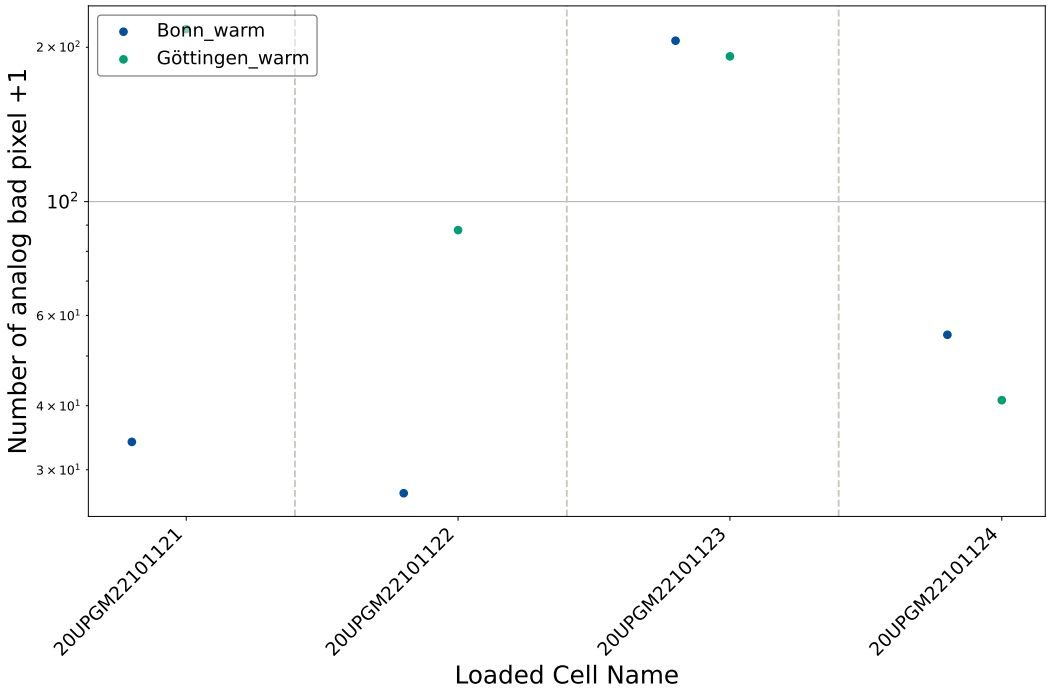


Figure 5.4: Comparison of the analog failing pixels per loaded module cell between Bonn and Göttingen with the serial number of the loaded module cell on the x-axis and the number of failing pixels on the y-axis.

closely aligned to the center of the module, where most hits are detected.

All pixels marked in red are pixels detecting more hits then visualized by the color bar. From these pixels the cross dividing the module in the four readout ASICs is the most prominent, stretching to the edges of the module. This is due to the larger edge pixels on the sensor tile between the readout ASICs as explained in Section 3.2, hence these pixels also detect a larger number of hits than all other pixels. This is also the case for the pixels directly beneath the source.

From these source scans a disconnected bump map can be created, by marking all pixels with less than 5% of the mean occupancy, described in Section 3.2.1, as disconnected and the numbers for this cuts are shown in Table 5.1. When comparing the cut values to the source scan occupancy maps, it can be found, that the cut is chosen conservatively enough to not consider a pixel beneath a SMD as disconnected. Disconnected pixels are usually at around 10 hits per pixel, while the cuts are at about 4 hits per pixel.

From these cuts, the disconnected bump maps can be created and a comparison between Bonn and Göttingen for the Loaded Cell 121 is shown in Fig. 5.7. When comparing the two maps the areas of the disconnected bumps are similar in place and size. This shows that both scan methods find a similar area of delamination, with similar results for the other Loaded Cells.

To further compare the areas, the number of disconnected bumps is displayed in Table 5.2. For both measurements the number of disconnected bumps is comparable, which, combined with the maps, confirms that the disconnected bumps measured in Göttingen are truly disconnected.

When layering the disconnected bump maps and the module flex of the module, as done in Fig. 5.8, it can be found that the delamination areas are underneath the pick-up points of the module flex. For a Loaded Cell, the wirebond protection canopies are glued to these points. Therefore, a possible

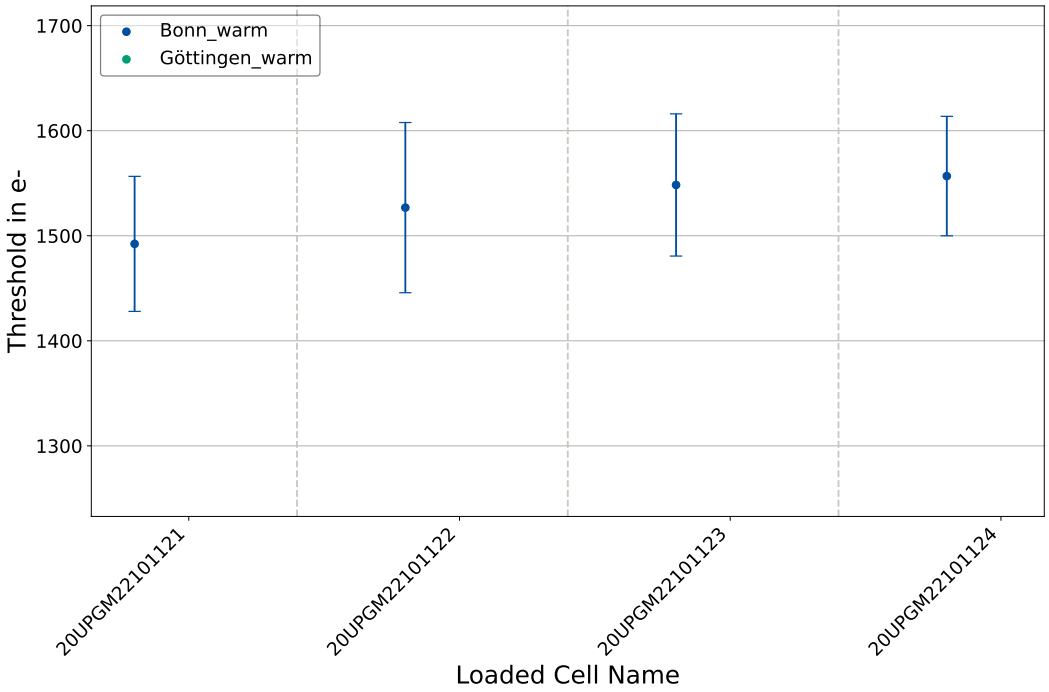


Figure 5.5: The mean and the standard deviation for a whole Loaded Cell tuned to 1 500 e^-, which is calculated from a gauss-fit to the threshold distribution with the Loaded Cells from Göttingen on the x-axis and the threshold in e^- on the y-axis.

Loaded Cell	Readout ASIC	No. of hits	mean hits	No. hits <5% cut
121	0x15997	16495178	107.4	5
121	0x159ab	14692484	95.7	4
121	0x159d9	12800881	83.3	4
121	0x159a3	14645527	95.3	4
122	0x159c4	12335451	80.3	4
122	0x159a4	10673188	69.5	3
122	0x15998	11493398	74.8	3
122	0x159ac	12115010	78.9	3
123	0x159c5	14035372	91.4	4
123	0x159a5	11854271	77.2	3
123	0x15999	13390687	87.2	4
123	0x159ad	13155855	85.7	4
124	0x159c8	13450371	87.6	4
124	0x159a7	12089933	78.7	3
124	0x1599b	11862934	77.2	3
124	0x15993	12118159	78.9	3

Table 5.1: Number of hits and the resulting cut values to create a disconnected bump for the Loaded Cells.

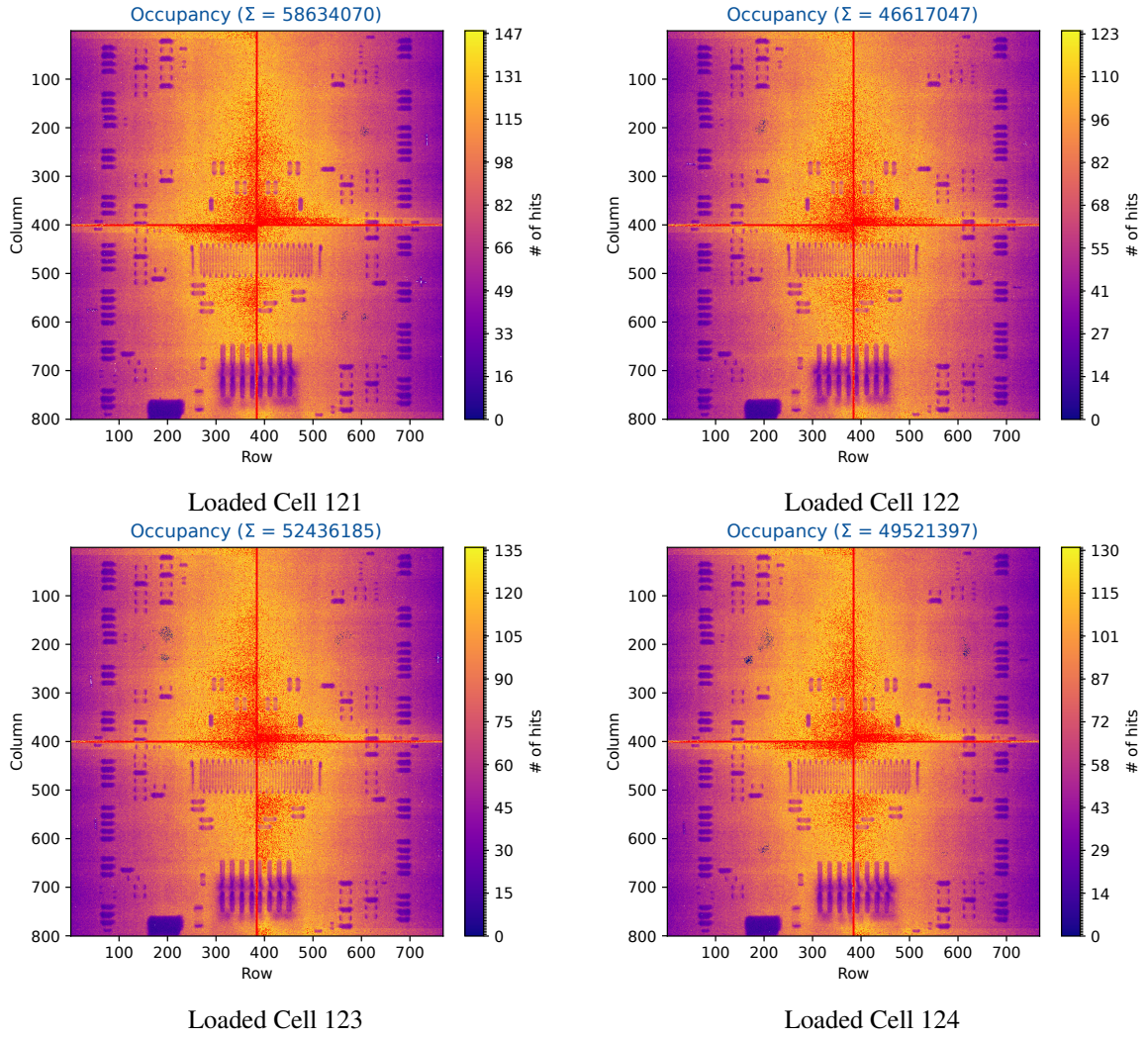


Figure 5.6: Source scans of the four Loaded Cell illuminated for two hours with ^{241}Am.

Module	Number of thermal cycles	Disconnected bumps measured in Göttingen	Disconnected bumps measured in Bonn
121	350	471	222
122	700	219	128
123	350	381	403
124	550	510	486

Table 5.2: Number of disconnected bumps in similar areas measured in Bonn and Göttingen in comparison.

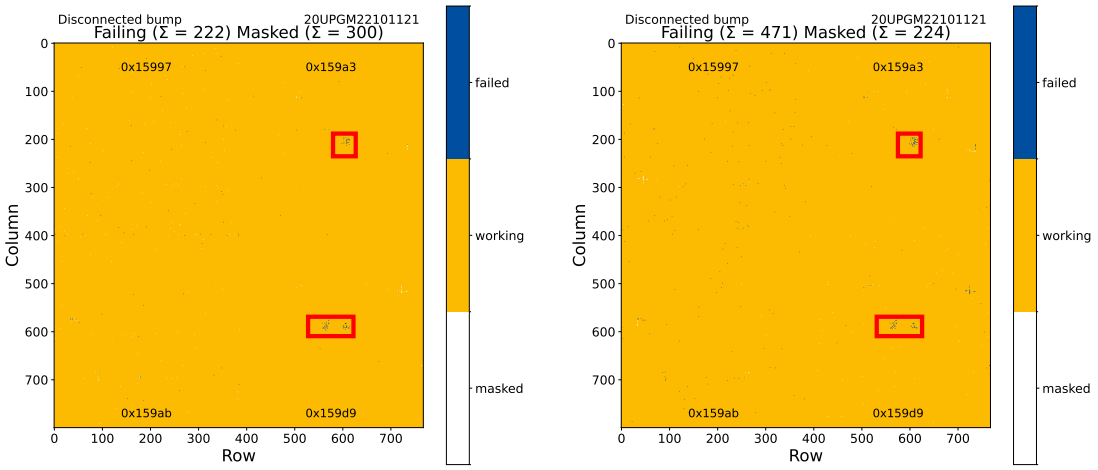


Figure 5.7: Disconnected bump maps from Bonn (left) and Göttingen (right) for module 121, with the same pattern of disconnected bumps, marked by the red rectangles.

explanation for the delamination of these bump bonds is, that they get weakened when the ITk Pixel module gets picked up, or mounted with the canopies and are susceptible to delamination. In general such a delamination is highly undesirable for an ITk Pixel module, but the minimum number of thermal cycles that each Loaded Cell underwent is 350 as can be seen in Table 5.2. Therefore, the first delamination areas occur at a three times higher amount of thermal cycles, than a typical ITk Pixel module is expected to receive in the detector. This concludes, the temperature changes in the ITk can result in such delaminated areas on some ITk Pixel modules, but within the expected lifetime of the ITk, this will pose no risk to the operation of the detector.

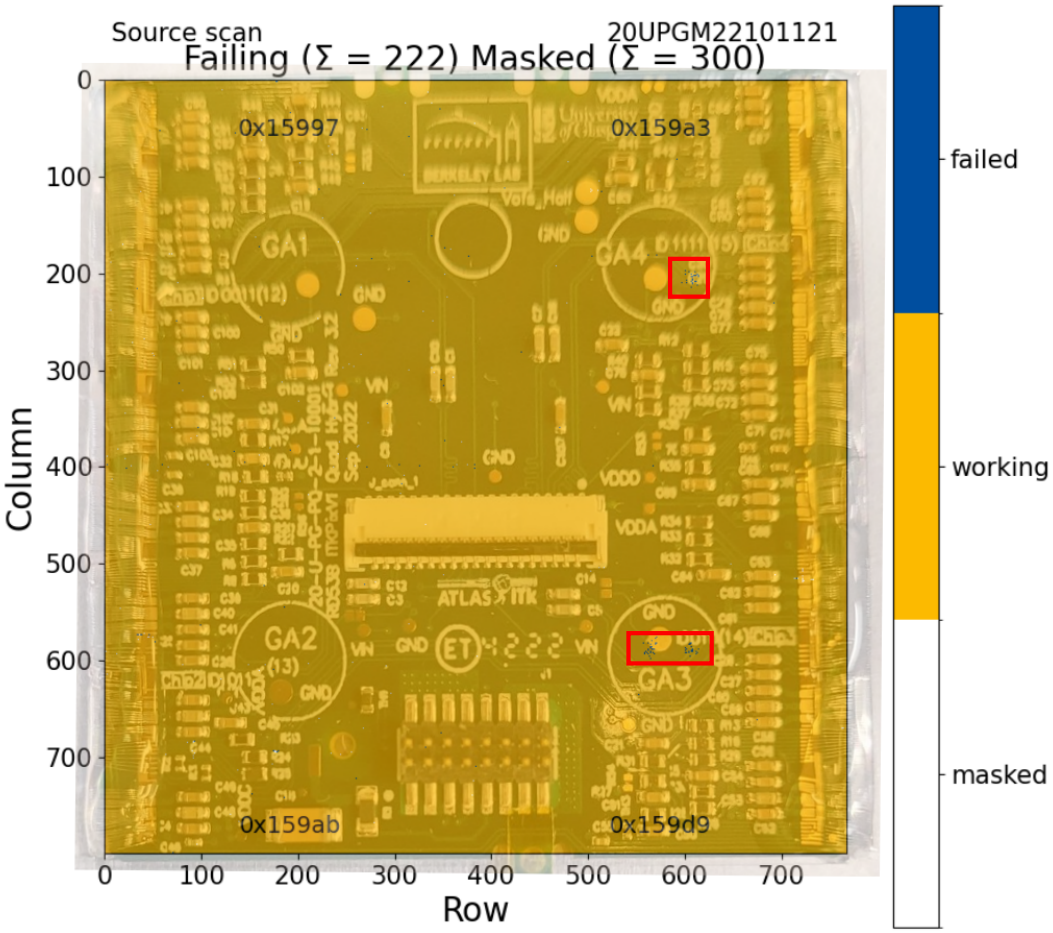


Figure 5.8: Disconnected bump map of Loaded Cell 121 layered with the module flex of the ITk Pixel module, with red rectangles highlighting the disconnected bumps.

CHAPTER 6

First pre-production Half-Ring

The University of Bonn is a Cell Integration site and is expected to produce 30-50 Loaded Local Supports for the ATLAS ITk in the coming years. For this venture the construction and testing structures were setup over the last years to prepare for the integration of a Loaded Local Support. One step in this preparation for the production is the construction of a pre-production Loaded Local Support. The Cell Integration site in Bonn was ready for such a task in November of 2024. At a similar time the parts for the first pre-production Layer 3 Half-Ring of the collaboration were ready and the Cell Integration site in Bonn received the order to assemble it.

A Layer 3 Half-Ring contains 22 Loaded Cells distributed between 2 SP chains as explained in Section 3.3. With only 12 Loaded Cells from Japan being available at the time, only one SP chain was populated on the Half-Ring, which requires 11 Loaded Cells on a Layer 3 Half-Ring leaving one as a spare.

To test the whole production chain, the 12 Loaded Cells went through the standard Module QC testing procedure, described in Section 3.4, for a Loaded Cell in Japan creating the configurations, which will be used at the other sites to test them. After this they were shipped to CERN, where the standard production chain was deviated from to perform an additional Loaded Cell reception for most Loaded Cells to check if the shipment from Japan to CERN created any problems and grade the Loaded Cells for Longeron and Inclined Half-Ring pre-production. Afterwards the Loaded Cell and the Functional Local Support were shipped to Bonn for the Cell Integration. In Table 6.1 the performed scans for each Loaded Cell are shown, until the Loaded Cell reception in Bonn and the known errors from the previous testing sites. Here the most notable error comes from the core columns, which are explained in Section 3.1 and need to be deactivate completely if broken.

Serial number	Shortened name	Testing steps	Known errors [33]
20UPGM22601095	095	Module QC Loaded Cell reception CERN Loaded Cell reception Bonn	broken columns
20UPGM22601133	133	Module QC Loaded Cell reception CERN Loaded Cell reception Bonn	
20UPGM22601134	134	Module QC Loaded Cell reception CERN Loaded Cell reception Bonn	broken core column
20UPGM22601139	139	Module QC Loaded Cell reception Bonn	
20UPGM22601140	140	Module QC Loaded Cell reception CERN Loaded Cell reception Bonn	
20UPGM22601141	141	Module QC Loaded Cell reception CERN Loaded Cell reception Bonn	broken core column
20UPGM22601145	145	Module QC Loaded Cell reception CERN Loaded Cell reception Bonn	
20UPGM22601150	150	Module QC Loaded Cell reception CERN	Two broken readout ASICs Only delivered as spare
20UPGM22601151	151	Module QC Loaded Cell reception Bonn	
20UPGM22601152	152	Module QC Loaded Cell reception CERN Loaded Cell reception Bonn	One broken readout ASIC two broken core columns
20UPGM22601157	157	Module QC Loaded Cell reception Bonn	
20UPGM22601177	177	Module QC Loaded Cell reception CERN Loaded Cell reception Bonn	broken core column

Table 6.1: Loaded Cells with the naming scheme used in this thesis, testing stages performed and known issues.

6.1 Cell Integration process

The Cell Integration is a four step process consisting out of

- Loaded Cell reception,
- pigtail assembly,
- Loaded Cell integration on LLS,
- LLS electrical QC.

The Loaded Cell reception as a first step has the purpose of checking the Loaded Cells on their functionality after the transport from the Cell Loading sites to the Cell Integration sites. After unpacking, the received Loaded Cells go through a visual inspection, a high voltage leakage current scan like for the validation of the Loaded Cell QC Box Section 4.3 and a Pixel Failure Analysis (PFA), that consists out of a digital, analog, threshold, disconnected bump and merged bump scan. These tests check if the Loaded Cells still fulfill the requirements for the ITk Outer Barrel. After a Loaded Cell passed the reception tests, the final production pigtail is installed. After connection, a glue dot is placed on the pigtail to act as a strain relief for the connectors.

Having assembled an adequate number of Loaded Cells for the to be integrated LLS the Cell Integration can start. This process starts with cleaning the Base Blocks on the Functional Local Support with isopropanol alcohol. After this thermal paste is applied to the Base Blocks to guarantee a good thermal contact between the Base Block and the Cooling Block. Now the Loaded Cells with the Cooling Block on the backside can be screwed to the Functional Local Support. The last step to complete a LLS, is to connect these single Loaded Cells to the PP0, as explained in Section 3.3.

With the LLS assembled the electrical testing of the whole structure can begin. Here a visual inspection, HV leakage current scan of each HV chain, a PFA and a measurement of the voltages and currents on the Loaded Cells are run in warm and cold conditions, which translates to a sensor and readout ASIC temperature of 20 °C for warm and 0 °C to −10 °C for cold tests. If all Loaded Cells on the LLS still show similar results as in the Module QC and Loaded Cell reception the LLS is successfully integrated. If a result differs from the previous tests, the problem can be investigated and in the worst case a Loaded Cell assembled on the LLS could be exchanged. In the end the assembled and tested LLS is transported to CERN to be integrated into the ITk Outer Barrel.

6.2 Loaded Cell reception of the pre-production Half-Ring

In this Section the procedure [34] and testing for the Loaded Cell reception of the first pre-production Half-Ring is described.

6.2.1 Testing procedure

The Loaded Cells arrive in a module carrier as shown in Fig. 6.1, that is wrapped into an electrically shielded foil. After unpacking the Loaded Cell, the first step is the visual inspection.

Here the Loaded Cell is checked for mechanical damages like ripped wire-bonds, a good position of the wire-bond protection, damages to the module flex, broken pins of the Cooling Block or in general larger contamination like dust. In the production this step will be done with a photograph and an assisting

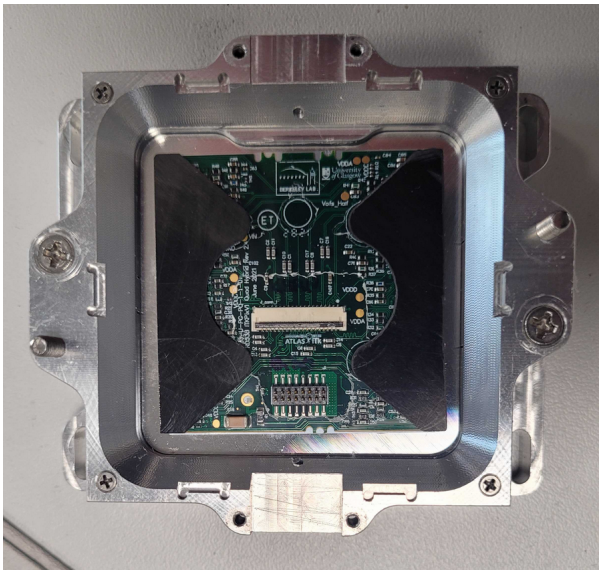


Figure 6.1: Loaded Cell from the top in module carrier.

analysis software, which will upload the picture to the production database and guides the tester through the visual inspection. In the pre-production this was not possible, as no program for the Loaded Cell reception existed to go through this procedure and no camera setup was prepared. Therefore, this step was done manually and the different parts were checked by eye.

As a next step the data and power pigtail needs to be connected to the Loaded Cell as shown in 6.2 wearing gloves and a grounding strap. With the Loaded Cell ready to be tested in the Loaded Cell QC Box, one of the aluminum jigs is prepared with thermal paste to create a better thermal contact between the jig and the carrier. Afterwards the Loaded Cell is placed on the jig and the pigtails are connected to the data and power adapter boards, as shown in Section 4.2.

Now the Loaded Cell QC Box gets closed and flushed with dry air, until a dew point of at least $-20\,^{\circ}\mathrm{C}$ is reached. When this is the case, the cooling is activated and the Loaded Cell is cooled to $10\,^{\circ}\mathrm{C}$ and then the LV is turned on. After this power-up the Loaded Cell should typically dissipates a power of about 10 W as described in Section 4.2. With the Loaded Cell now powered the cooling needs to be adjusted to hold the sensor and readout ASICs at $(20 \pm 4)\,^{\circ}\mathrm{C}$. This first power-up is with no HV applied to safeguard the sensor.

If the LV runs with the correct amount of power and the temperature has settled, the HV leakage current scan is started. For this an IV curve of the sensor is measured were the bias voltage is increased from 0 V to -200 V in 5 V steps with a settling time of 5 s.

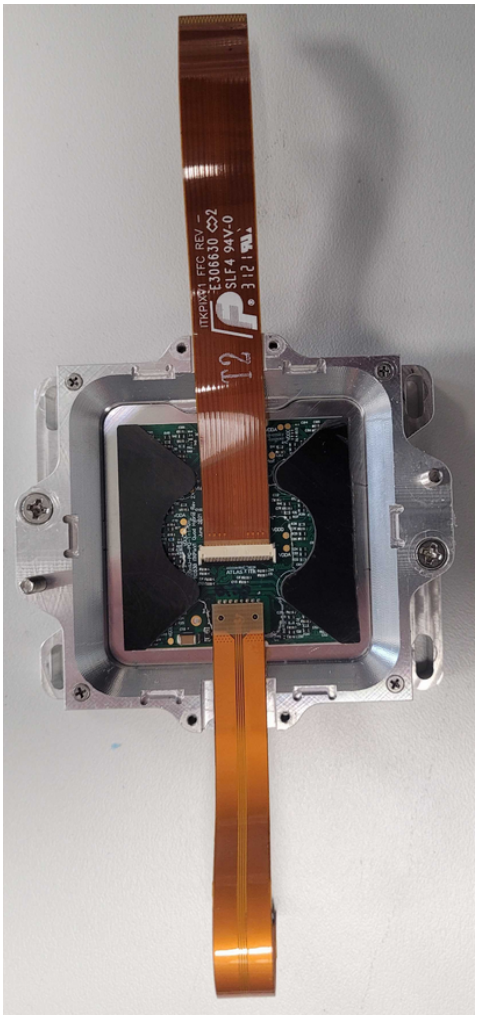


Figure 6.2: A Loaded Cell from the top with separated data and power pigtail installed.

As a next step a full PFA is performed, with the configurations from the Module QC site, but without the pixel mask. Here the pass criteria for a Loaded Cell in the Loaded Cell reception are:

- Total number of failing digital/analog pixel less than 0.1% per module, totaling to 614 failing pixels each.
- Threshold scan less than 1% failing s-curves and mean threshold $(1\,500 \pm 100)\,\mathrm{e}^-$ with less than $50\,\mathrm{e}^-$ dispersion.
- Excessive noise ($> 300\,\mathrm{e}^-$) from threshold scan for less than 1% of the pixels.
- Total number of disconnected bumps less than 0.1% per module, totaling to 614 failing pixels each.
- Total number of merged bumps less than 0.1% per module, totaling to 614 failing pixels each.

With these criteria the Loaded Cells can be marked as passed or failed. For the Loaded Cells delivered for the pre-production Half-Ring, these margins were not applied, because the 12 Loaded Cells that were available had problems like broken core columns or readout ASICs.

As a last step before the Loaded Cells are ready for integration on the Half-Ring, the temporary pigtails need to be removed, because on the Half-Ring the final detector pigtails are used.

6.2.2 Results of the Cell Reception for the pre-production Half-Ring

In a standard Loaded Cell reception the goal is to find Loaded Cells, that do not fulfill the criteria to be integrated onto a LLS and discard them. For the pre-production the goal is a different one, as it serves to ensure and validate if the production process is under control. Therefore the Loaded Cells are compared to the previous tests done in Japan and at CERN to find if the transportation, module handling and testing procedure meet the high standards for the ITk Outer Barrel and do not damage the Loaded Cells in the process. To test this, also Loaded Cells that do not met the pass criteria for the ITk Outer Barrel can be used as only their degradation throughout the process needs to be monitored.

Loaded Cell 150 showed the worst performance of the available Loaded Cells during Module QC and Loaded Cell reception at CERN. As only 11 of the 12 Loaded Cells were to be mounted on the Local Support, this Loaded Cell was kept as a spare and not fully tested.

Visual inspection

In the visual inspection of the 12 Loaded Cells no flaws or damages were observed. However, after the final pigtail installation, described in Section 6.3.1, bend wire-bonds were found on Loaded Cell 152, as visible in Fig. 6.3. As no pictures were taken in the visual inspection of the pre-production, it is unclear when the bending of the wire bonds happened. This problem and other concerns supported the conclusion that an automated visual inspection process with pictures is necessary during production for the Loaded Cell reception.

HV leakage current

The first performed electrical scan for each Loaded Cell is the HV leakage current scan, which measures an IV curve of the sensor. For the tests with the Loaded Cell the leakage current should be lower than 100 μA and not exceed the breakdown voltage.

An example for such an IV curve is shown in Fig. 6.4. In this IV curve the standard diode like behavior of a silicon sensor can be observed, with the slowly increasing current, when the sensor is fully depleted, until the break down voltage at about 180 V. From these plots a working point for the Loaded Cells can be determined. This is important, because on the LLS the Loaded Cells are grouped into two HV groups, as explained in Section 3.3. For this the working points should not be to far apart, to have all Loaded Cells in the HV chain with a fully depleted sensor, as the HV supplied can vary with the position on the PP0 and a small added up current consumption for each HV chain.

The division in two HV groups on the PP0 for the Half-Ring can be found in Table 6.2. All of the used Loaded Cells have their plateau in the same voltage area and therefore, as a voltage reference, 80 V was chosen. With the voltage set for the HV chain, the grouping was decided from the leakage current.

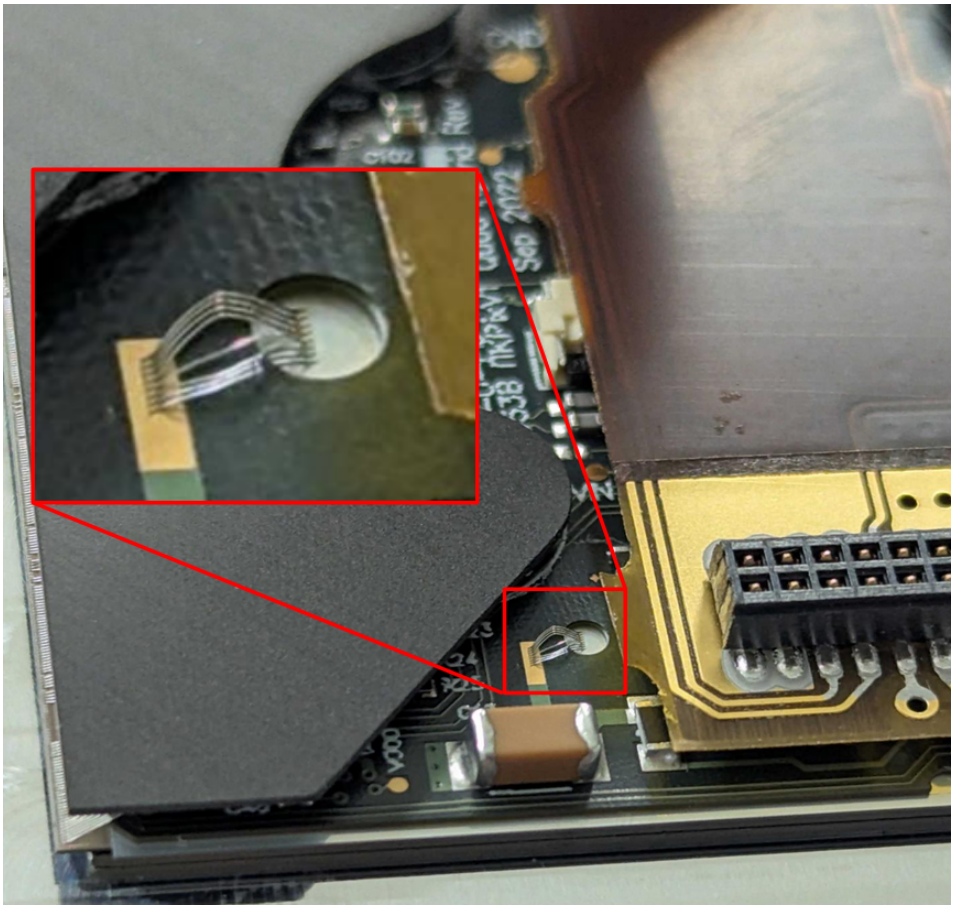


Figure 6.3: Front side of the Loaded Cell 152 with zoom on the still functional but unusually bend HV wire bonds.

	139	140	141	145	152	177	095	133	134	151	157
I in μA	0.05	0.05	0.14	0.06	0.05	0.17	0.05	0.05	0.05	16.7	0.06
Group	1	1	1	1	1	1	2	2	2	2	2

Table 6.2: Sensor leakage currents of the Loaded Cell at 80 V bias voltage and grouped in the two HV groups on the Layer 3 Half-Ring.

Pixel Failure Analysis

The full PFA was run for the 11 Loaded Cells determined for the Half-Ring. For the spare Loaded Cell 150 a digital and analog scan was performed, to find out how bad the damages to the readout ASICs are.

The scan results of this can be found in Fig. 6.5. To run the two scans the readout ASIC three and four needed to be deactivated as well as a core column on readout ASIC one, as all of these caused to many data errors to successfully run the scans with 150. This also shows the reason why it can only be used as a spare, because on the Half-Ring the modules need to be tested with data merging, which sends out all data collected by the Loaded Cell over the readout ASIC four. Therefore having a readout ASIC that needs to be fully masked as the only directly accessible readout ASIC on the Half-Ring is a risk.

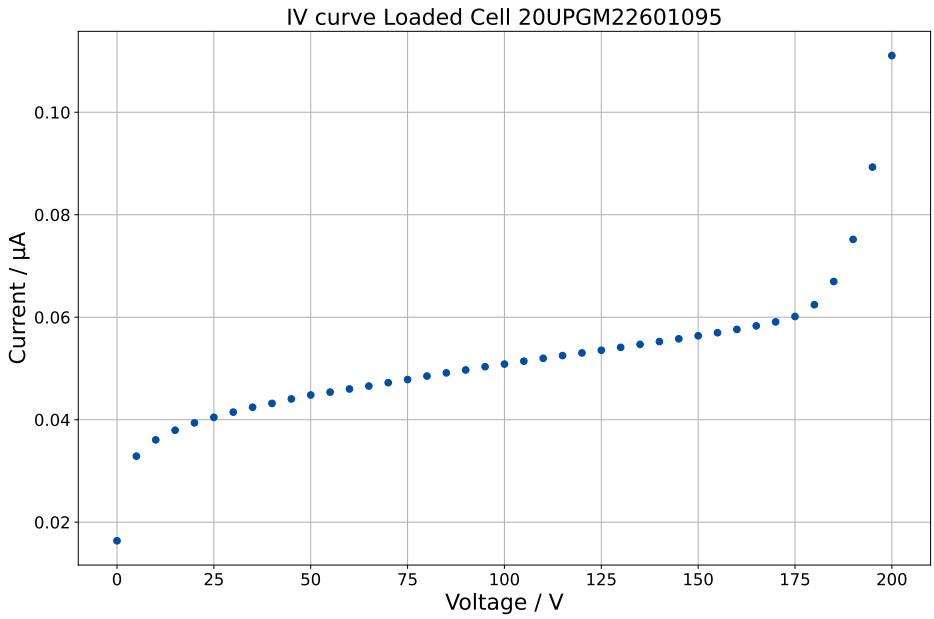
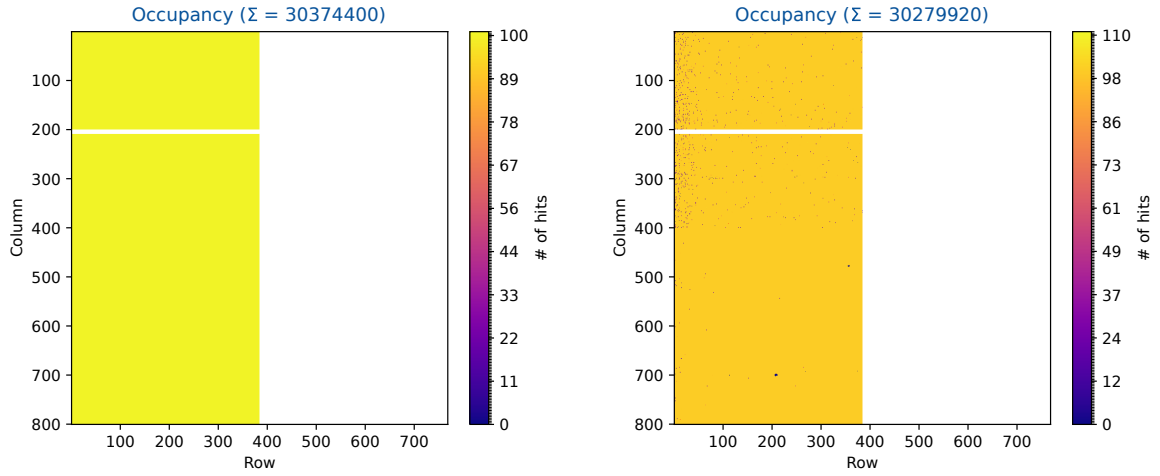


Figure 6.4: An IV curve from the sensor of the Loaded Cell 095 supplied with a voltage up to 200 V measured in 5 V steps.



(a) (b)

Figure 6.5: Combined module occupancy map of a digital scan from 150 (a). A combined module occupancy map of a analog scan from 150 (b), both with two chips and a core column masked to be able to run scans without data transmission errors.

Therefore it was not tested any further.

Another necessary information to understand the scan results of the Loaded Cell reception is that a malfunction of the utilized database, which is not the final production database, lead to the usage of untuned configurations for the Loaded Cell 152. This was only found out after the scans were finished

and the Loaded Cell was already in the pigtail installation, therefore the scan results cannot be sensibly compared to the Module QC, which uploaded the scan data for the tuned Loaded Cell 152.

The first performed scan in a PFA is a digital scan. The comparison of the failing digital pixels from the three testing stages performed in Japan, CERN and Bonn, for each Loaded Cell can be seen in Fig. 6.6. In general all Loaded Cells show a similar amount of digital bad pixels at all three testing sites.

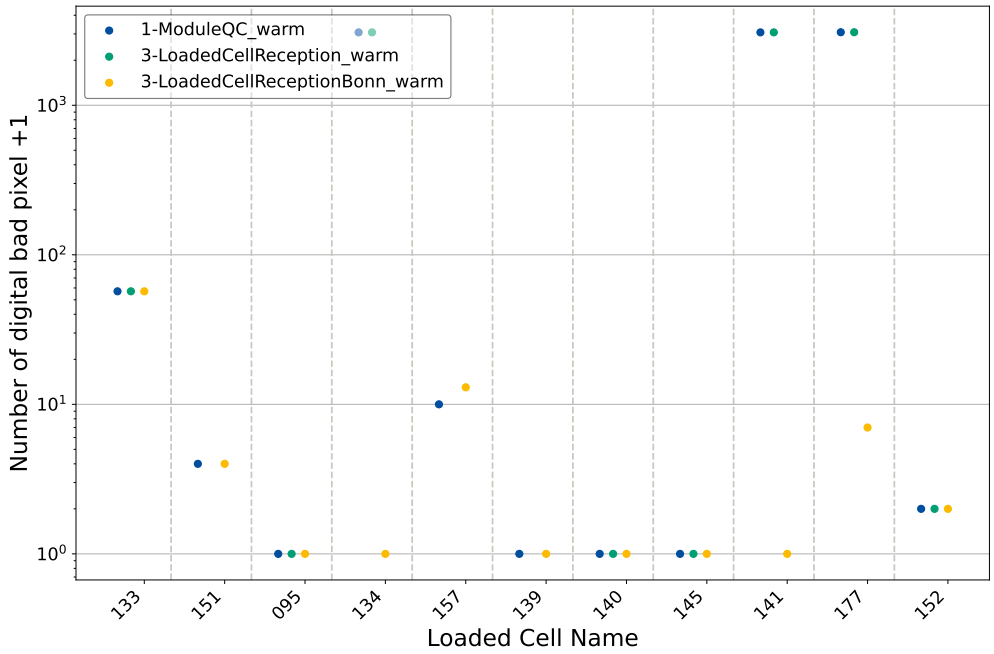


Figure 6.6: Comparison of the digital failing pixels per Loaded Cell between the three sites Japan (ModuleQC), CERN (LoadedCellReception) and Bonn (LoadedCellReceptionBonn) with the Loaded Cells on the x-axis and the number of failing pixels on the y-axis in log scale.

Nevertheless it can be seen that some of the Loaded Cells have several broken pixels, like the Loaded Cells 134, 141 and 177 with over 3000 digital failing pixels. These Loaded Cells have a broken core column that is deactivated before the digital scan, because such a column can lead to data transmission errors, which would render a scan useless. For this reason these columns cannot detect any injected hits in Japan and at CERN and show a high amount of failing digital pixels. At Bonn the core columns got deactivated and additionally masked for the digital scan and therefore also detect no hits. However, in the analysis a mask for a pixel removes it as a failing pixel and therefore the deactivated core columns do not show up in Bonn. An example for a deactivated core column can be found in Fig. 6.7.

For the analog scan similar data of the failing pixels are shown in Fig. 6.8. Here the fluctuations between the sites are larger, but this is expected as an analog scan is much more susceptible to noise and as the masks got reset for the PFA a difference in failing pixels at around 10 pixels per Loaded Cell can be expected. In general this is no problem, as long as the criteria of 0.1% failing pixels per Loaded Cell is not breached.

For the Loaded Cell 095 two columns are analog broken amounting for 768 bad pixels, which were masked before the analog scan in Bonn, but not in Japan or at CERN. Similar on Loaded Cell 133 a broken core that was masked in Japan and at CERN was not masked in Bonn amounting for an additional

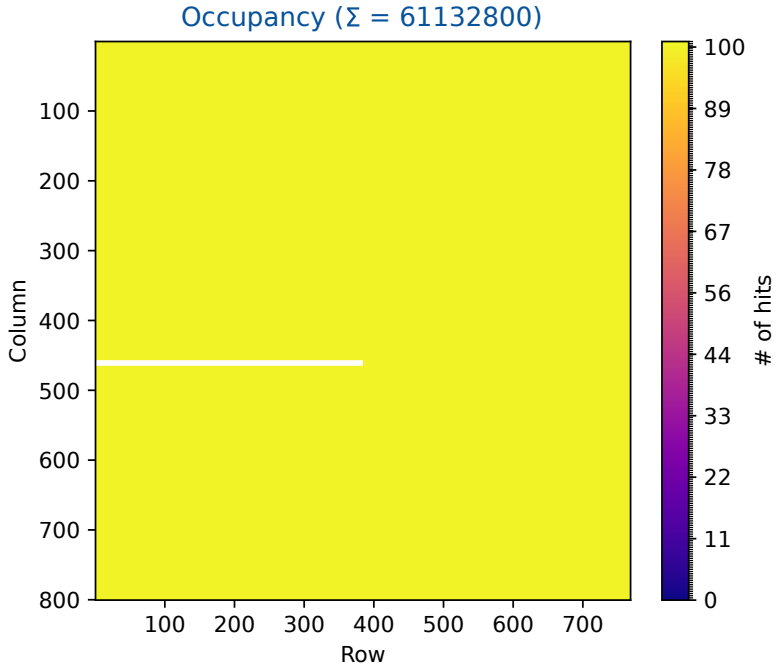


Figure 6.7: A combined module occupancy map from a digital scan of the Loaded Cell 141 with a deactivated core column on one readout ASIC

64 failing pixels in Bonn. The last problematic Loaded Cell is 152, which for CERN and Bonn shows more than 153600 analog failing pixels. This amount of failing pixels comes from the readout ASIC three, which is broken and does not respond. In Japan this whole readout ASIC got masked for the analog scan, but not for CERN and Bonn leading to the high amount of failing pixels.

From the threshold scan a mean threshold and noise in units of electrons can be calculated as shown in Section 3.2.1. This result can be seen in Fig. 6.9 and Fig. 6.10. Here the mean threshold and noise is displayed with the error bar corresponding to one standard deviation of the underlying gauss distributions as explained in Section 3.2.1. For threshold and noise the scans show comparable result for each site and Loaded Cell in the mean and width of the distribution. Only the untuned Loaded Cell 152 shows a much higher mean threshold and dispersion at Bonn and CERN, as expected for an untuned Loaded Cell. Here the noise is much more important, as the tuning has almost no influence on the noise of each pixel. This can also be seen for 152, as the noise is in all scans at the same level, showing that the Loaded Cell 152 is still in a similar condition, as in the Module QC.

An in-depth analysis of this scan can be done with a failing s-curve analysis. the result of this is shown in Fig. 6.11. In addition to the mean threshold and noise of the scan this analysis shows that only for a small portion of pixels no s-curve can be fitted. This is important, because a similar mean for the threshold and noise could also be calculated with half the number of pixels, but it would be less accurate and not comparable to scans made with more successfully fitted s-curves. It should be noted, that for almost all Loaded Cells there are more failing s-curves in Bonn than at the other sites. This can come from various effects, but the most likely one is that the other sites use YARR as a readout system, while Bonn uses BDAQ. In both systems the fitting algorithm is slightly different as YARR is programmed in C++, while BDAQ is programmed in Python. Also for the failing s-curves the Loaded Cell 152 shows

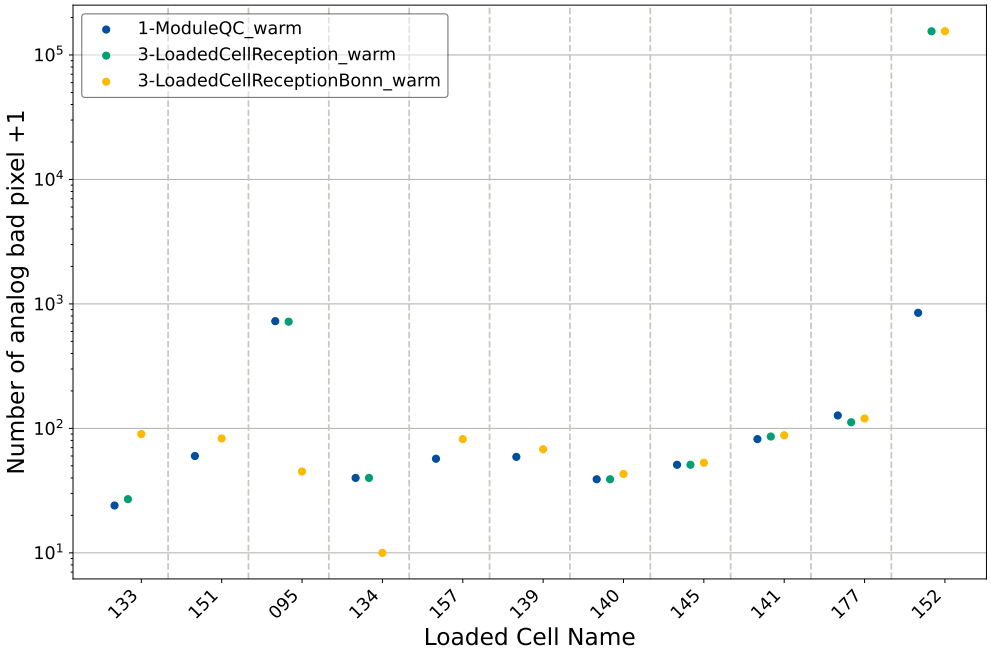


Figure 6.8: Comparison of the analog failing pixels per Loaded Cell between the three sites Japan (ModuleQC), CERN (LoadedCellReception) and Bonn (LoadedCellReceptionBonn) with the Loaded Cells on the x-axis and the number of failing pixels on the y-axis in log scale.

the 153600 failing pixels from the unmasked third readout ASIC and therefore only the tuning of the three other readout ASICs is depicted in the threshold and noise scan.

The next scan in the PFA is a merged bump scan and the compared number of merged bumps for each module can be found in Fig. 6.12. Here almost no fluctuation between the sites is visible and even for 141 and 177, which have the largest difference between the sites, it is less than 11 pixels per Loaded Cell. This amount is, similar to the fluctuations in the analog scan, negligible.

In Fig. 6.13 the comparison for the number of disconnected bumps can be found. Here it needs to be stated, that the disconnected bump scan done in Japan and at CERN are through the cross talk method, while the disconnected bump scans performed in Bonn are with the source scan method, which are both described in 3.2.1. For most Loaded Cells this leads to similar results and a number of disconnected bumps below the threshold.

Nevertheless on Loaded Cell 133 the disconnected bumps number is at about 1800 disconnected bumps in Bonn, while only 10 are found at the other sites. Here the problem resulted from the different methods used. The self trigger source scan showed, that the deactivated broken core on the Loaded Cell breaks the whole core column. The broken core in the analog scan and the core column in the self trigger source scan can be found in Fig. 6.15.

For Loaded Cell 177 no result is shown for the Loaded Cell reception in Bonn, because no self trigger source scan was possible with this Loaded Cell. The reason for this is an overflow of data from the Loaded Cell to the readout system, as it would usually happen for a noisy or stuck pixel constantly sending data and overloading the system, but in this case no noisy or stuck pixel could be found on the Loaded Cell after repeated scans. Therefore a random trigger source scan instead of a self trigger

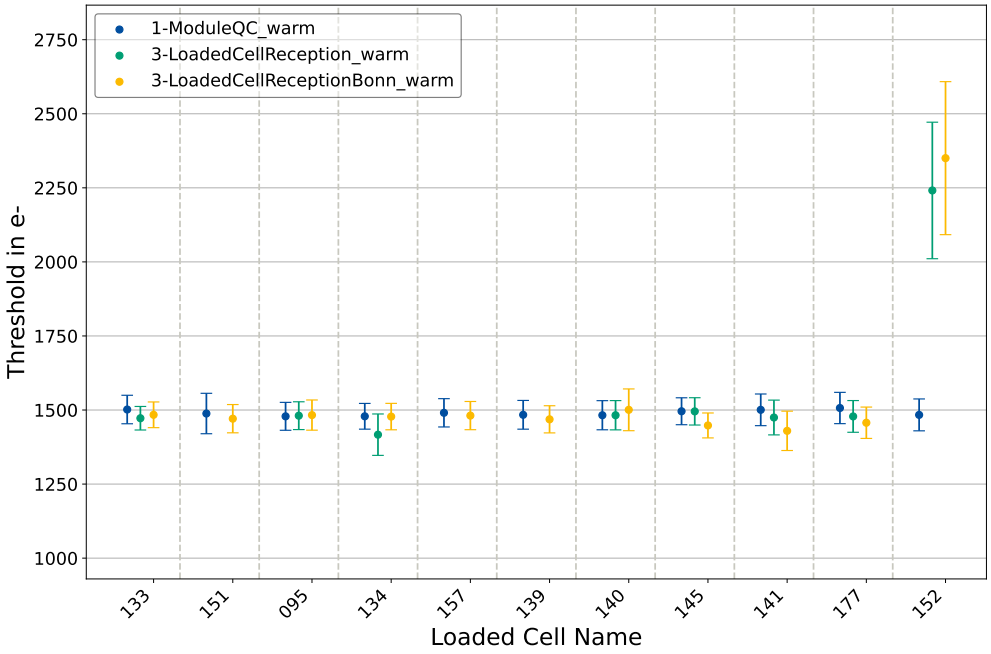


Figure 6.9: Mean threshold of a whole Loaded Cell calculated from a gauss-fit to the threshold distribution and compared between the three sites Japan (ModuleQC), CERN (LoadedCellReception) and Bonn (LoadedCellReceptionBonn) with the Loaded Cells on the x-axis and the threshold in number of electrons on the y-axis.

scan was used, which instead of letting the Loaded Cell trigger by itself, sends a trigger signal to the Loaded Cell from the BDAQ board. As these triggers are not synchronized to the pixels being hit, as in the self trigger source scan, it is called random trigger source scan. This scan results in a much lower hit rate, than a self trigger source scan, as only hits get detected that coincide with the trigger signal. The comparison of a self trigger source scan used for a usual disconnected bump analysis and a random trigger source scan can be found in Fig. 6.14, where the difference in hit rate is obvious, even though the random trigger scan ran for more then double the time of the self trigger source scan.

With the low hit rate of the random trigger source scan a disconnected bump analysis is not possible, because every pixel with less hits then 5% of the mean occupancy is considered a disconnected bump, which in this case would be all pixels with zero hits, resulting in almost all pixels underneath a SMD being considered disconnected. Therefore the analysis of the disconnected bumps is skipped for this Loaded Cell. As well as for the other scans the Loaded Cell 152 is an outlier in the disconnected bump scan. For this scan the mask was not applied in Japan and resulted in more than 153600 disconnected bumps, which all come from the broken third readout ASIC.

All these data show that the disconnected bumps scan via cross talk is a good enough measure to test the disconnected bumps. Nevertheless a self trigger source scan should be conducted to catch cases of Loaded Cells like 133 and 177, which underwent all tests with no problems, but failed to detect particles.

In Summary the Loaded Cell reception tests showed no performance degradation due to transport of the Loaded Cells from CERN to Bonn and 11 Loaded Cells were chosen to populate the Half-Ring.

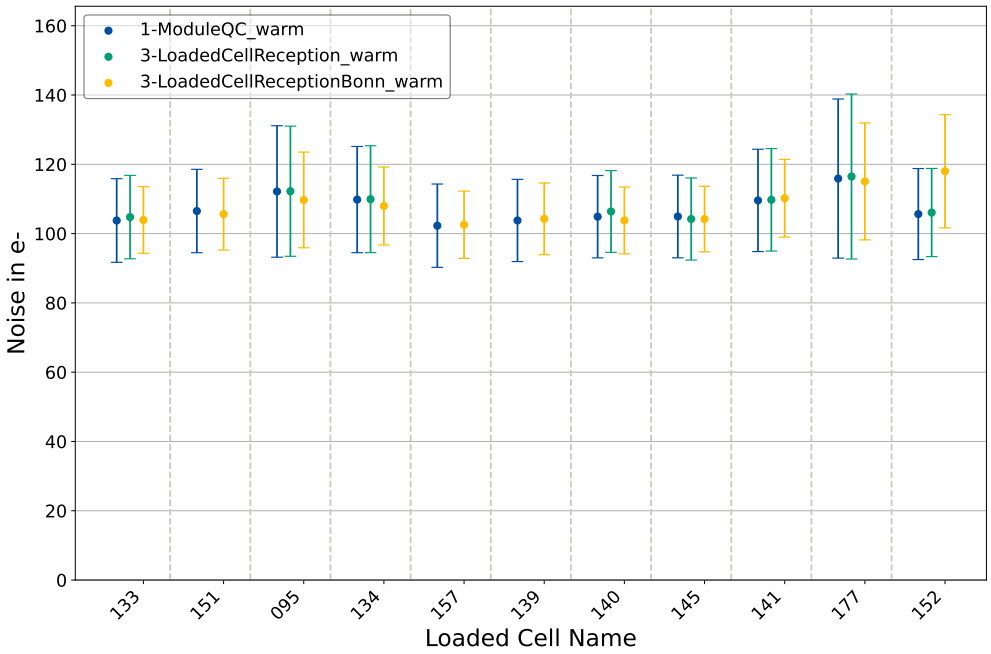


Figure 6.10: Mean noise of a whole Loaded Cell calculated from a gauss-fit to the noise distribution and compared between the three sites Japan (ModuleQC), CERN (LoadedCellReception) and Bonn (LoadedCellReceptionBonn) with the Loaded Cells on the x-axis and the threshold in number of electrons on the y-axis.

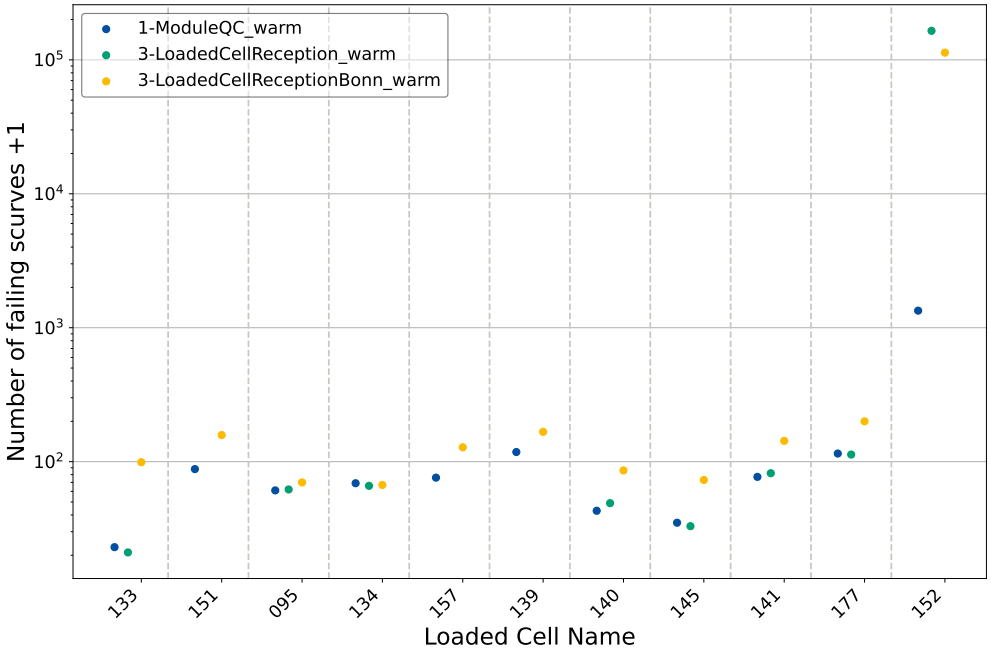


Figure 6.11: Number of failed s-curves per Loaded Cell between the three sites Japan (ModuleQC), CERN (LoadedCellReception) and Bonn (LoadedCellReceptionBonn) with the Loaded Cells on the x-axis and the number of failing s-curves on the y-axis in log scale.

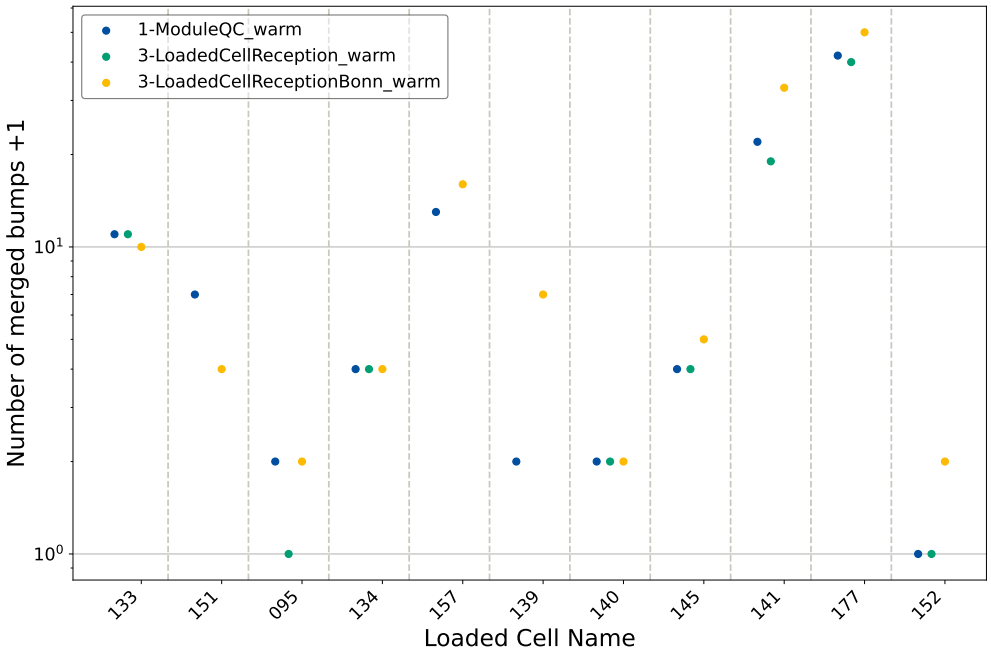


Figure 6.12: Comparison of the merged bumps per Loaded Cell between the three sites Japan (ModuleQC), CERN (LoadedCellReception) and Bonn (LoadedCellReceptionBonn) with the Loaded Cells on the x-axis and the number of merged bumps on the y-axis in log scale.

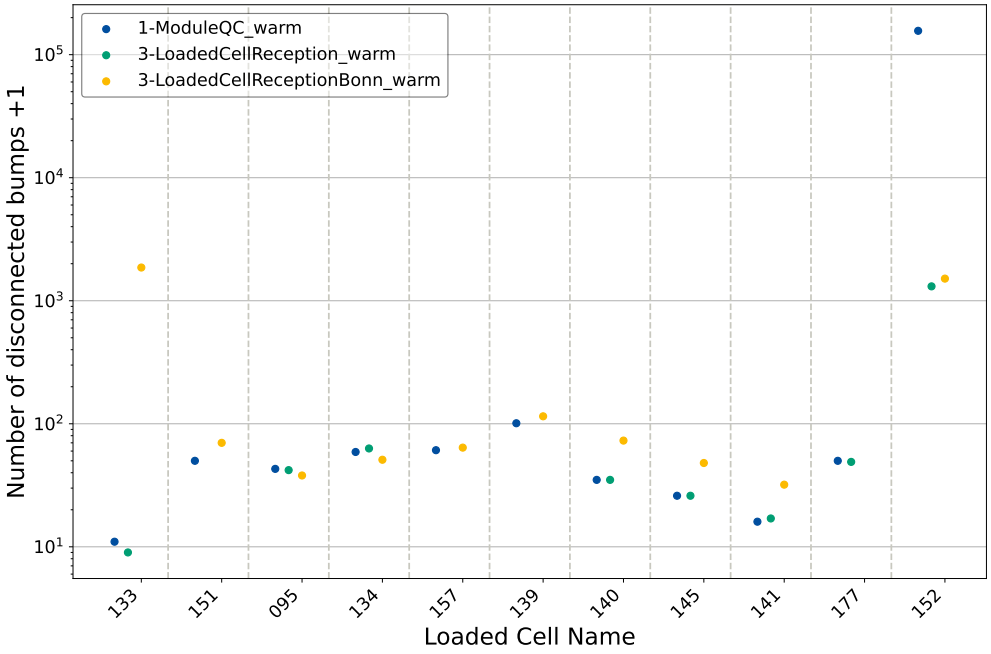
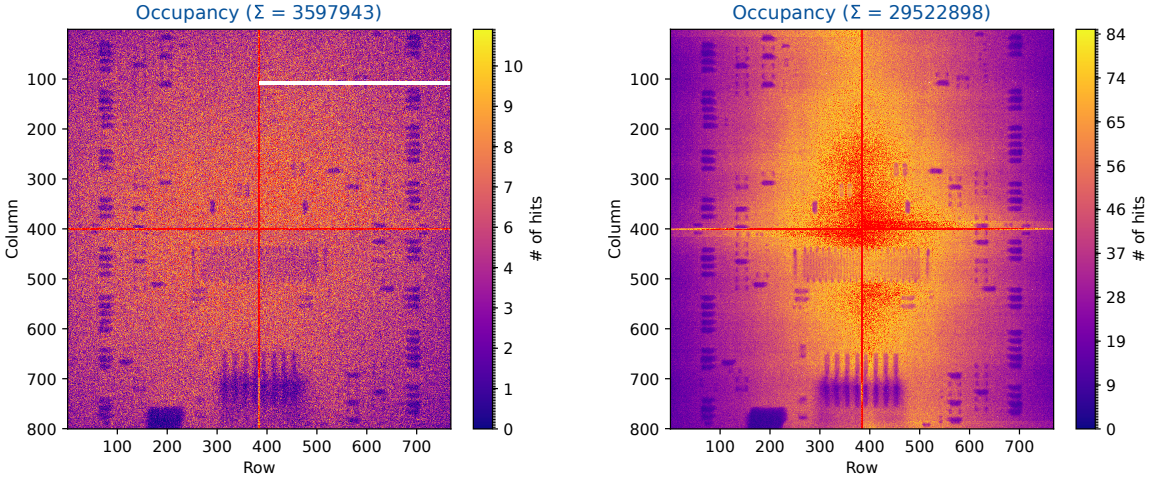
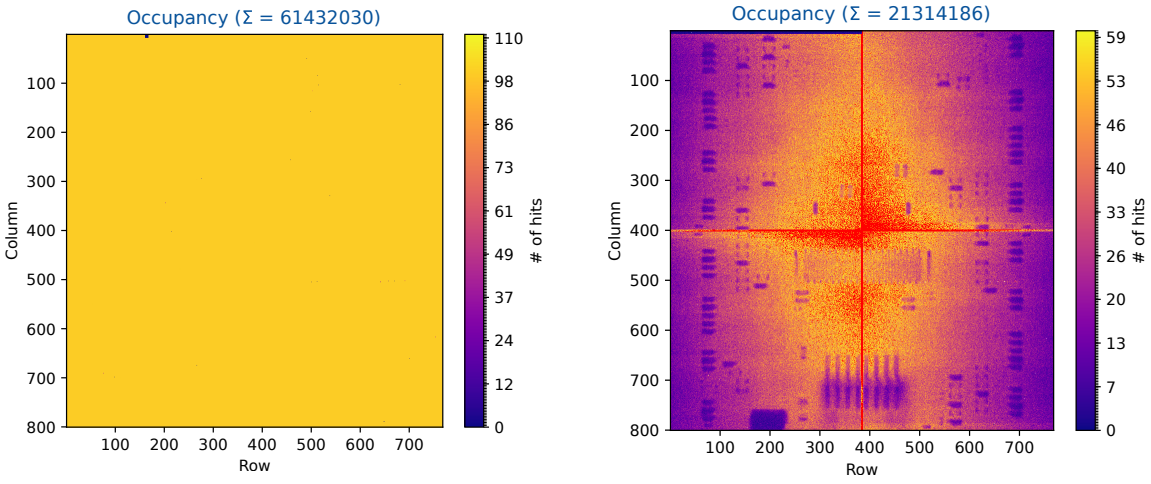


Figure 6.13: Comparison of the disconnected bumps per Loaded Cell between the three sites Japan (ModuleQC), CERN (LoadedCellReception) and Bonn (LoadedCellReceptionBonn) with the Loaded Cells on the x-axis and the number of disconnected bumps on the y-axis in log scale.



(a) (b)

Figure 6.14: Combined module occupancy map of a random trigger source scan from 177 run for two and a half hours (a). A combined module occupancy map of a self trigger source scan from 145 run for one hour (b). Both irradiated with ^{241}Am.



(a) (b)

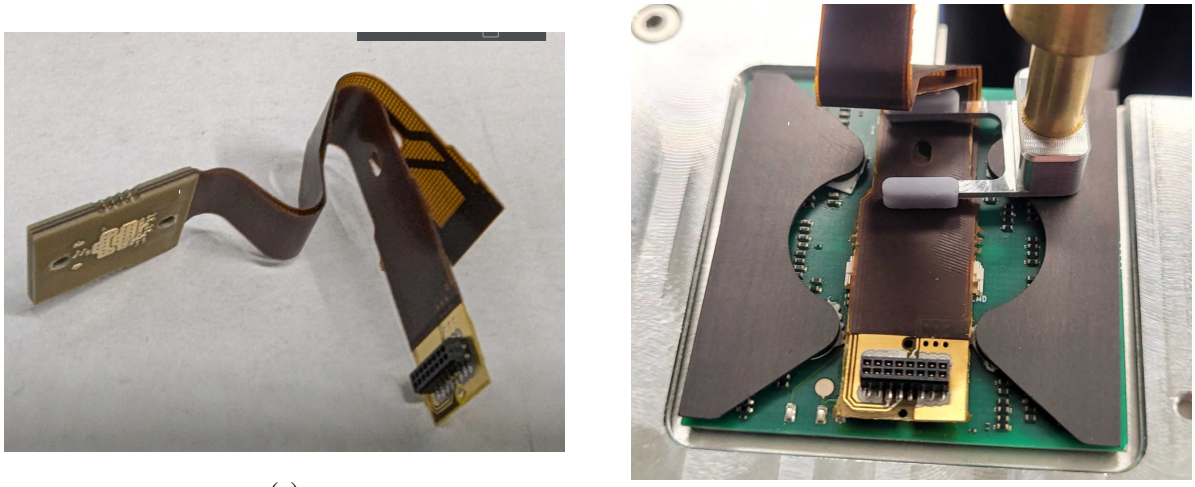
Figure 6.15: Combined module occupancy map of an analog scan from 133 with the broken core (a) and the combined module occupancy map of a self trigger source scan from 133 with the whole column not detecting hits after irradiation with ^{241}Am (b).

6.3 Mechanical Cell Integration

After successful testing of the Loaded Cells and guaranteeing that all of them arrived in similar conditions as originally tested in Japan, the mechanical integration of the Half-Ring can proceed.

6.3.1 Assembly of final pigtails to the Loaded Cell

The first step of the Cell Integration is the installation of the final pigtail. A back side pigtail for the Half-Ring and the pigtail installation tool are shown in Fig. 6.16.



(a) (b)

Figure 6.16: The final detector pigtail with data and power pigtail combined (a). Loaded Cell in the pigtail installation tool with the strain relief hole ready to be glued to the Loaded Cell (b).

The first step is to weight the Loaded Cell and the pigtail, for which the Loaded Cell is taken out of the carrier with a vacuum fork. Then the Loaded Cell is placed in the pigtail installation tool [35], where it is secured with vacuum. Then the pigtail can be installed, by first connecting the data pigtail and afterwards connecting the power pigtail. When the pigtail is connected a two component glue dot is put into the hole of the pigtail, gluing it to the Loaded Cell and acting as a strain relief for the connectors. To place the glue dot a syringe is used and the excess glue is put into a small bowl to check if it hardens correctly.

During the gluing a small air bubble can form within the glue. To get rid of it, a needle is used to stir the glue to let the air escape. After this the combined Loaded Cell and the pigtail are weight, to show that the glue dot weighs about 0.05 g. The result of this measurement is shown in Fig. 6.17. It can be observed that some glue dots seem to have negative weights and that the whole distribution is spread out. As adding a glue dot can not result in a weight loss, this behavior was not expected. The problem is that the available scale used for the measurement is not well suited for such low masses, as it has only an readability of 0.01 g and a linearity of ±0.03 g [1], which is close to the mass difference that shall be measured and could lead to the spread and negative measurement values. Also the measurements are

[1] Link to the datasheet of the scale https://www.kern-sohn.com/cosmoshop/default/pix/a/media/TPCB%201200-2-A/TD_PCB+1000-2_en.pdf

taken at least one day apart from each other as the glue hardens, which slightly changes the environmental conditions and could lead to small differences in the measurement.

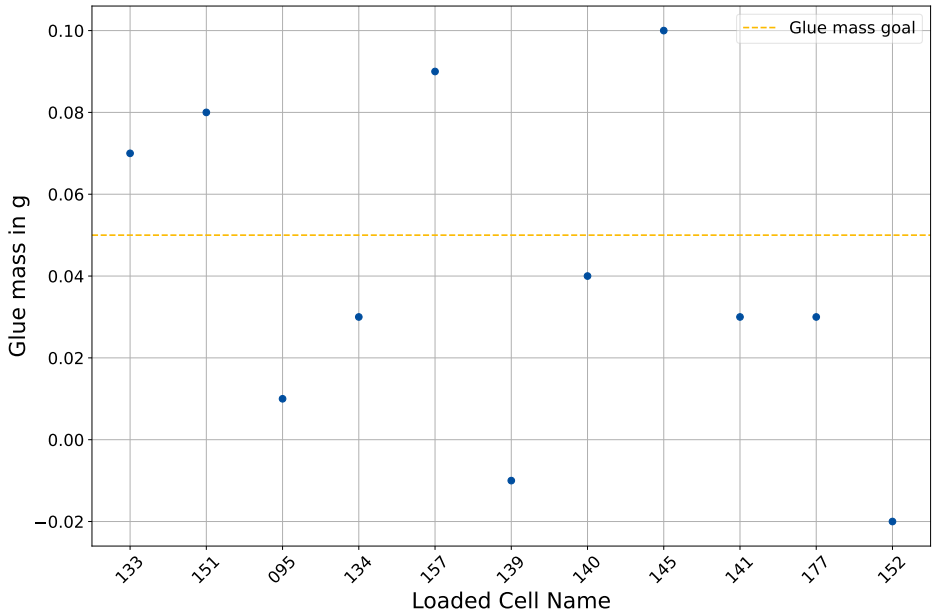


Figure 6.17: Calculated mass of the strain relief glue dot on each Loaded Cell for the pre-production Half-Ring.

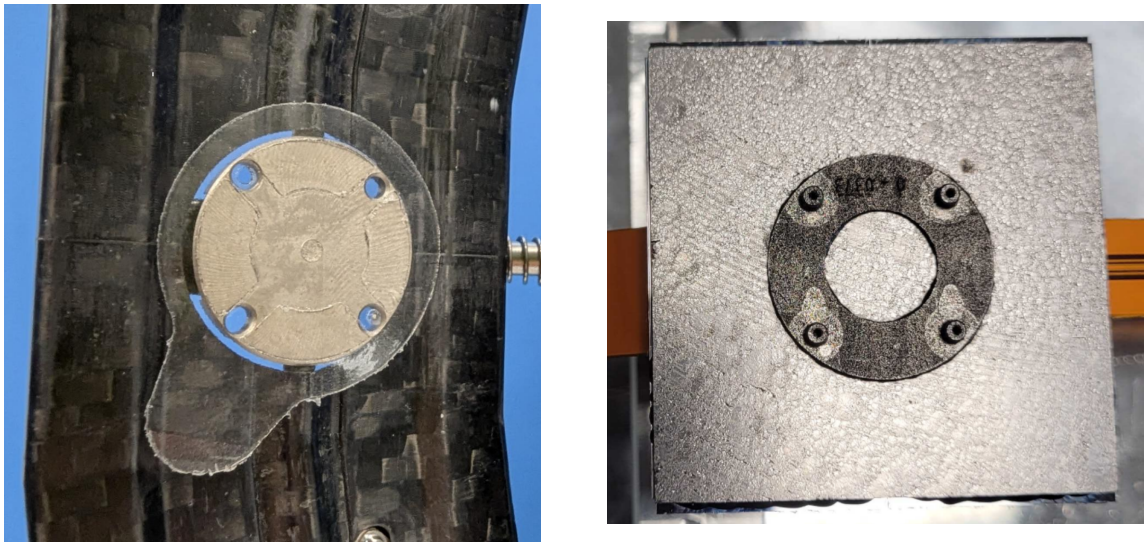
The whole gluing and curing process takes roughly one day for each Loaded Cell and with two available tools for the pigtail installation the gluing takes the longest time in the process of the Cell Integration. For the Layer 3 Half-Ring a total of 11 pigtails needed to be installed. It was decided to install SP chain two of the Half-Ring, which needs 5 Loaded cells with front side and 6 Loaded Cells with back side pigtails.

The only notable problem in this process was the differently bend pigtails delivered to Bonn, which was not optimal and resulted in differently bend pigtails for each Loaded Cell. This behavior can lead to problems in the installation of the SP chain on the Half-Ring and a bad metrology of the Half-Ring.

6.3.2 Cell Integration on the Half-Ring

After the glue for the strain relief hardened, the Loaded Cells can be integrated on the Half-Ring. As explained in Section 3.2, the Loaded Cell is connected to the Half-Ring by screwing the Cooling Block to the Base Block. To make the thermal interface between the two components, as good as possible, a thermal paste is applied. For this purpose a foil is placed on the Base Block, to cover the holes and the excess parts, where the Cooling Block does not touch the Base Block. The two components and the Base Block with the foil can be seen in Fig. 6.18. When the foil is well aligned the thermal paste is applied with a spatula and the result can be found in Fig. 6.19, for two Base Blocks with the foil removed and one with the foil and the excess thermal paste still covering the Base Block.

With the thermal paste applied to all Base Blocks, the Loaded Cells with pigtails can be integrated and screwed to the Half-Ring. This task is difficult, as the insertion of the four pins of the Cooling Block through the holes in the Base Block without touching or compromising the distribution of the thermal



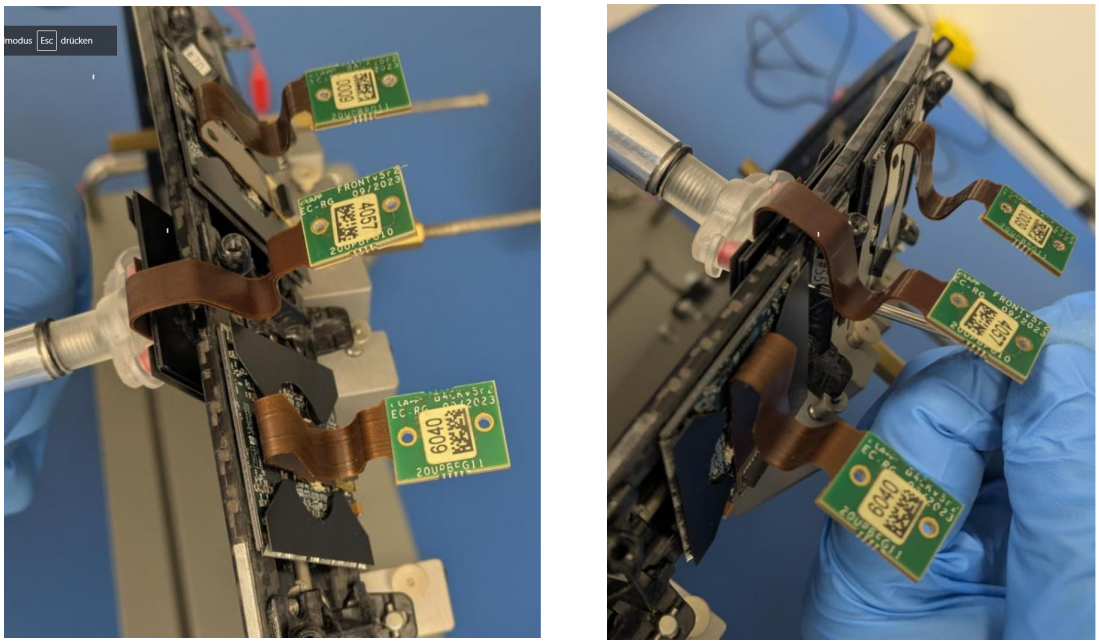
(a) (b)

Figure 6.18: The Base Block on the Half-Ring and covered with foil for the thermal paste application (a). A Loaded Cell from the back side with the Cooling Block visible as a counter part to the Base Block (b).

Figure 6.19: Front side of the Half-Ring with the Base Blocks covered with thermal paste with and without the thermal paste cover foil removed.

paste on the Base Block is not easy. Therefore this is a two person job, one holding the Loaded Cell with a vacuum fork, while being guided though the holes by the other person, who afterwards screws the Loaded Cell to the Half-Ring. This process can be seen in Fig. 6.20, where the front side Loaded Cells are already integrated and one back side Loaded Cell is in the process of integration.

When all Loaded Cells are integrated, the PP0 is connected to the support frame of the Half-Ring and bend in a circular shape. For each pigtail connection an interposer is placed with tweezers on the PP0, where the screw hole pins hold it in place. To do so the pigtail needs to be bend away a bit to have enough



(a) (b)

Figure 6.20: Integration of a Loaded Cell to the Half-Ring. One person holding the Loaded Cell in place with a vacuum fork, while the other one screws it to the Half-Ring in picture (b).

space to operate, because some pigtails were bend badly as explained in Section 6.3.1. This process gets more difficult the steeper the PP0 gets. With the interposer in place the pigtails get screwed to the PP0. The process of this installation can be seen in Fig. 6.21, where one pigtail is already connected, while one is in the process of installation, with the interposer hold in place and one pigtail still waiting to be connected. With all pigtails connected, the LLS is fully assembled and ready for the LLS QC.

6.4 Quality control of a Loaded Local Support

After the assembly of the LLS a QC process is performed with the tests described in Section 6.1, as it is still possible to re-work the LLS. Contrary to the other testing steps in the production of the LLS, no electrical QC of LLS was performed before within the Outer Barrel community, thus some procedures and steps of the electrical QC were not as solidified as for other steps in the ITk pixel detector production chain.

To test the LLS a quality control box was setup in Bonn, which is shown in Fig. 6.22. Here the pre-production Half-Ring is electrically and mechanically connected. The LLS supports can be placed like the pre-production Half-Ring in the example. To cool the LLS the MARTA CO_2 cooling plant is used, which is a two phase cooling system using CO_2 as a coolant. A characterization of this cooling plant is done by D. Hauner in [36]. To power the full LLS a LV power supply with four channels and a HV power supply with eight channels is setup to power the maximum number of four PP0s on a Longeron, which all have separate power lines. In the box a dew point of $-60\,^{\circ}C$ is mandatory for the testing with liquid CO_2. To reach this dew point pressurized dry air is used, which is dried to a dew

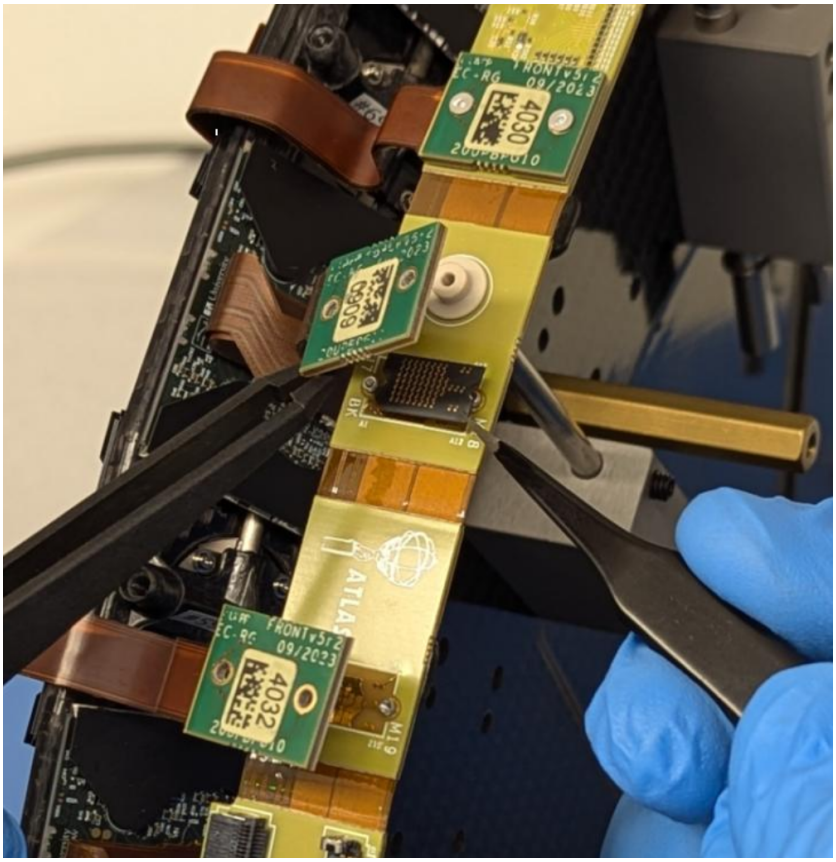


Figure 6.21: Installation of an interposer between the pigtail and the PP0 with the upper pigtail already connected and the lower one waiting for installation. Visible are the positioning holes, one interposer, the pigtails and a part of the PP0.

point of −70 °C with the dryer ATLAS Copco CD3[2].

To monitor all of the properties in the box an interlock system, which controls all the devices is implemented and an overview of some values is shown in Fig. 6.23.

To readout the LLS it was decided to use a system as close to the one in the final detector, to test the LLS under experiment conditions and because it is the only way to readout this many ITk Pixel modules. For this purpose the electrical signal of the Loaded Cells is transformed into an optical signal in the Optobox. From here it propagates through a fiber optic cable into the Felix server, which operates as the data acquisition system. On the Felix server the readout system YARR is installed. The construction, components and characterization of this test setup can be found in detail the thesis of A. Wald [37].

[2] Described in this product information https://www.atlascopco.com/content/dam/atlas-copco/compressor-technique/oil-free-air/documents/cd--bd--xd--series/2935362812_CDplus_BDplus_XDplus_leaflet_DE_Antwerp_LR.pdf

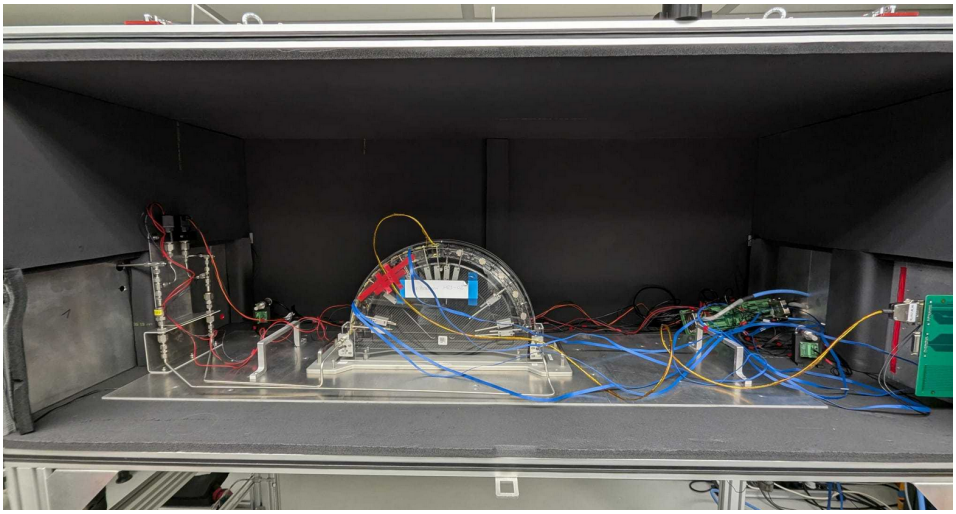


Figure 6.22: Half-Ring in the LLS QC Box.

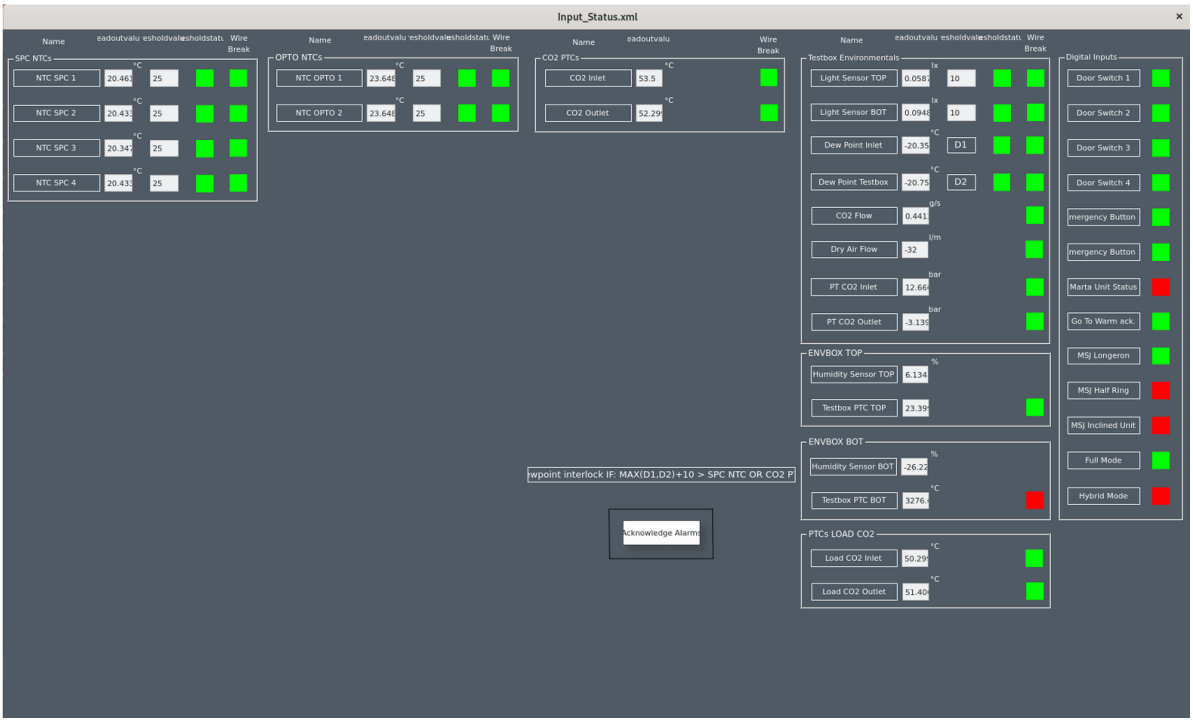


Figure 6.23: Overview of the readout sensors by the interlock of the LLS QC Box. In the left block one NTC of each SP chain is read out. In the middle the temperature of the Optobox and the temperature of the CO_2 outside of the box. In the right block the sensors in the box like light, dew point, CO_2 pressure and temperature, humidity and the digital running signals.

6.4.1 Testing procedure

To test a LLS the first step is to check if all of the data lanes of the Loaded Cells on the LLS are electrically connected. For this a device is connected to the readout chains and scans for the correct resistivity and capacity on the in- and output lanes. This confirms if a Loaded Cell is correctly connected. If this is the case the same number of in- and output lanes as there are Loaded Cells should be shown. This device can be seen in Fig. 6.24, where a dummy load is connected and all connections are measured as good.

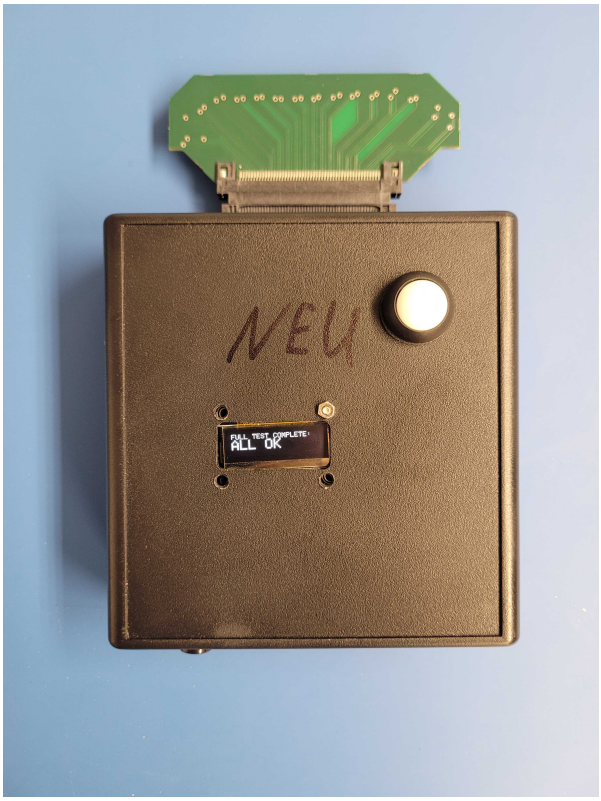


Figure 6.24: A device to test the readout connections on the LLS. Here connected to a dummy load, which simulates the connection and showing all possible connections are ALL OK.

After this test the LLS is connected to the LV, HV, readout and interlock system. Before power is supplied the temperature and voltage readings are checked as a sanity test to verify proper connection and functionality of the MOPS ASIC to each Loaded Cell. Similar to the device that checks on the readout connection, through the temperature readout it can be observed if all NTC readings show similar results and if the Loaded Cells are connected correctly.

After this the cooling can be turned on to get the Loaded Cells to around 10 °C, with no power switched on. If this temperature is reached on each Loaded Cell, the LV can be turned on. Each Loaded Cell should have a voltage drop of about 1.65 V at 5.88 A drawn, similar to the Loaded Cell reception. The first electrical testing cycle is performed in warm conditions, for which the cooling is adjusted accordingly to reach (20 ± 4) °C on each Loaded Cell as can be seen in Fig. 6.25.

In the standard procedure the LLS would be tested with data merging activated and all readout ASICs on one Loaded Cell read out over readout ASIC four. For the pre-production this testing cycle was first

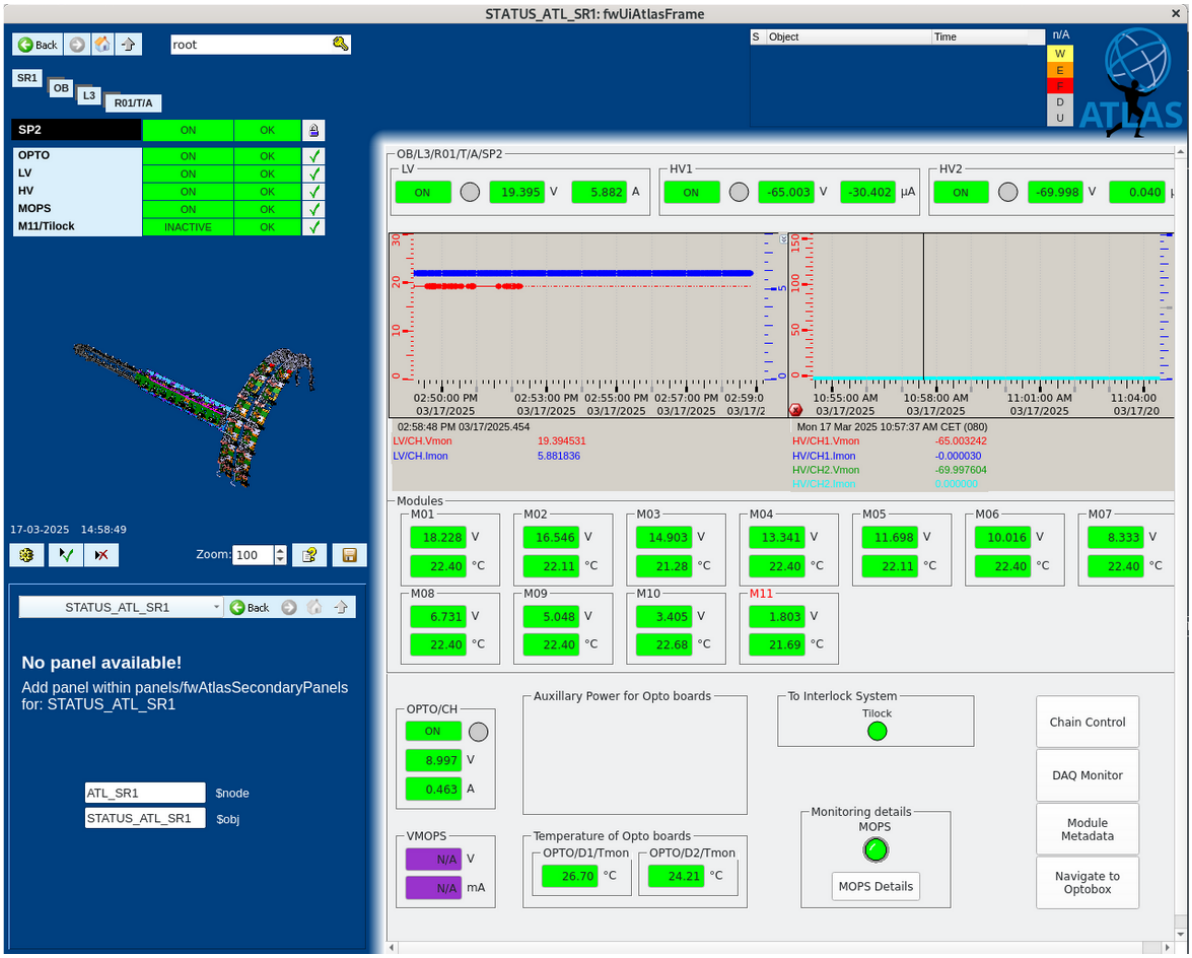


Figure 6.25: Control of the LV and HV chains on a Layer 3 Half-Ring and the temperature and voltage drop over each Loaded Cell.

only performed for the fourth readout ASIC on each Loaded Cell without data merging, because data merging is not well functioning and produces a lot of data errors. Nevertheless it was performed after the single readout ASIC test, as a separate testing cycle as the data errors usually accumulate on one readout ASIC, while the others produce useful data. All the performed electrical tests can be found in Section 6.1.

After completion of all electrical tests in the warm conditions, MARTA is cooled down to the lowest with MARTA possible temperature and another electrical testing cycle is performed. Again the tests start with a single readout ASIC measurement and are afterwards performed with data merging.

6.4.2 Overview over the results from the Half-Ring

A detailed account of the electrical QC setup, its commissioning and the results for the electrical QC of the Half-Ring can be found in the dissertation of Alexandra Wald [37]. Nevertheless some data were already available during the electrical testing. Here, only a first overview of the test results is briefly summarized.

The first conducted test was the test for the readout connection and here the problem evolved, that the device from Fig. 6.24 malfunctioned and produced no usable data. For this reason the device was send back to CERN and a new one was send to Bonn, which did not arrive early enough to have any use in the electrical testing of the Half-Ring and therefore the test was skipped. The next step is to connect the Half-Ring to all electrical devices and to the temperature readout, which showed that all Loaded Cell were connected.

Now the LV could be turned on and here it was found, that the last three Loaded Cell did not consume any power. A first visual inspection of the Loaded Cells did not reveal any obvious cause. Here the re-workability of the Half-Ring came in handy and the pigtails of the Loaded Cells could be disconnected from the PP0 to look for the cause of this behavior. It was found that during installation two interposers were badly connected and had bend teeth. For the third last position this caused a short circuit in the LV line, effectively bypassing three Loaded Cells in the serial powering chain. The current working hypothesis for this pattern is the position of the affected Loaded Cells on the Half-Ring, where the installation of the interposers is performed at close to a 90° angle with respect to the Cell Integration table. As such the interposers are not well secured on the PP0 and can easily rotate relative to the PP0 during pigtail connection, which can cause excessive stress on the spring connectors of the interposer. The broken interposers could be exchanged by two new ones making the Half-Ring fully functional, when it was turned on again. A proposed solution is to lift the Half-Ring on one side, to have the PP0 in a more level position, which makes installation easier.

The following electrical tests revealed no further obstacles. As one of the standard benchmarks, the result of a threshold scan of all Loaded Cells on the Half-Ring, is presented here and compared to the results from the Module QC and Loaded Cell reception, see also Section 6.2.2. In Fig. 6.26 the threshold and in Fig. 6.27 the noise for each Loaded Cell tested in the warm PFA of the electrical tests compared to the previous testing sites can be found. All of these data are taken from the measurement without data merging and therefore only represent readout ASIC four.

When comparing the thresholds and noise between the four different sites it can be found, that all Loaded Cells performed similar before and after the Cell Integration. With this information and the number of failing s-curves from Fig. 6.28, which also shows comparable results to the previous stages, it can be concluded that the Cell Integration worked reasonably well and no Loaded Cell got damaged in the process. In summary no performance degradation was observed during the electrical QC of the Half-Ring, which during the pre-production is equivalent to successfully passing the QC stage.

With the Half-Ring being assembled and fully electrically tested it was shipped to CERN for further tests, which also served as a trial run for the regular shipping of LLS to CERN during the production phase.

6.5 Summary of the pre-production Half-Ring

The pre-production of the first Half-Ring for the ATLAS ITk in Bonn was overall a success. The concept of the Loaded Cell reception and its procedures could be thoroughly test and validated. All of the 11 Loaded Cells foreseen for the Half-Ring went through the reception tests and showed that the precautions taken throughout the pre-production for the Loaded Cells protected them from damages during transport and assembly.

Also the pigtail installation could be tested and even though the pigtails that arrived were badly bend, the procedure of installation worked and showed no signs of failure.

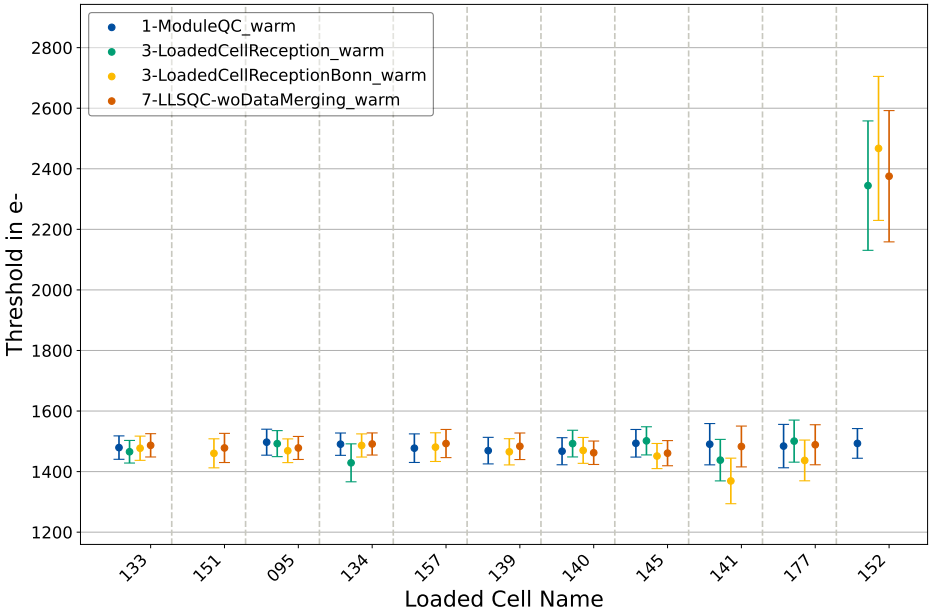


Figure 6.26: Mean threshold of the fourth readout ASIC from all Loaded Cells calculated from a gauss-fit to the threshold distribution and compared between the three sites Japan (ModuleQC), CERN (LoadedCellReception) and Bonn (LoadedCellReceptionBonn and LLSQC-woDataMerging) with the Loaded Cells on the x-axis and the threshold in number of electrons on the y-axis.

The last step, the Cell Integration, proved to be the most difficult part of the process. Here the integration on the Half-Ring itself with the application of the thermal paste, the screwing of the Loaded Cells to the Half-Ring and the installation of the PP0 is not a trivial task and requires significant coordination. A first potential problem in the Cell Integration work flow was found manifested in damaged interposers for the connection between PP0 and Loaded Cells. The damaged parts could be replaced without complications. For the underlying problem a hypothesis and potential solution was formed and has to be further investigated once additional Local Supports are available for Cell Integration.

In the end, the Half-Ring and with it the pre-production can be considered a successful test of the production line, with only small adjustments to be made for the production of the LLS is Bonn.

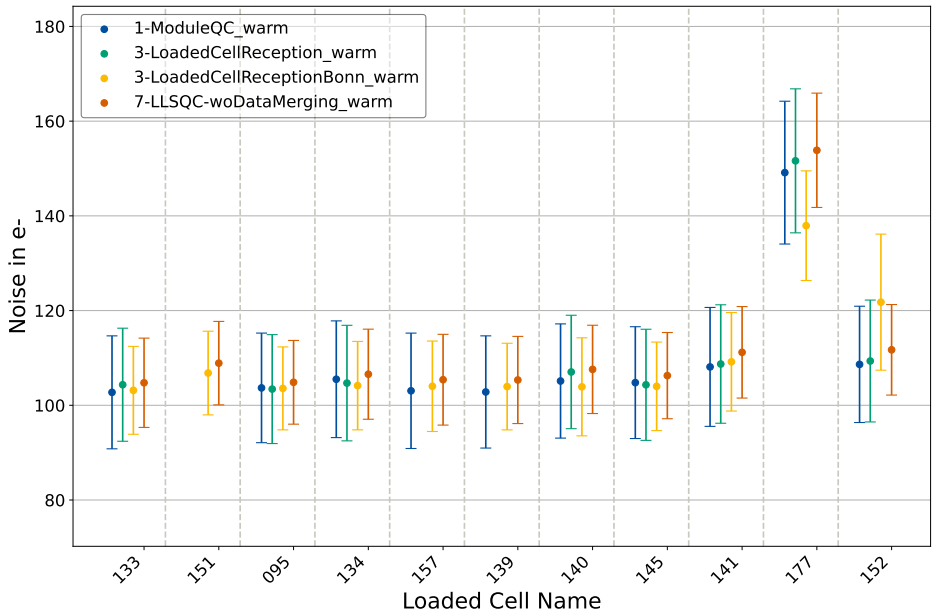


Figure 6.27: Mean noise of the fourth readout ASIC from all Loaded Cells calculated from a gauss-fit to the noise distribution and compared between the three sites Japan (ModuleQC), CERN (LoadedCellReception) and Bonn (LoadedCellReceptionBonn and LLSQC-woDataMerging) with the Loaded Cells on the x-axis and the threshold in number of electrons on the y-axis.

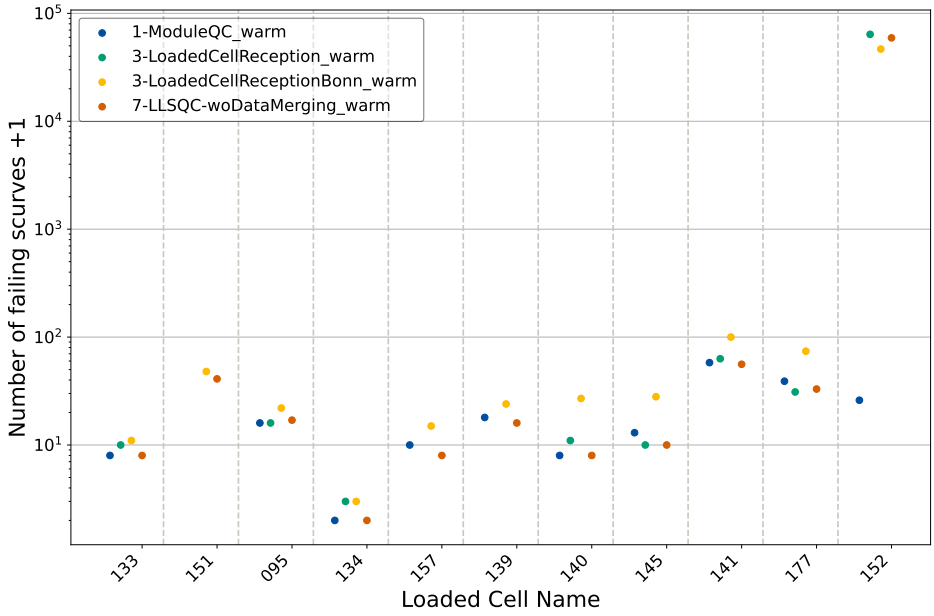


Figure 6.28: Number of failed s-curves of the fourth readout ASIC from all Loaded Cells between the three sites Japan (ModuleQC), CERN (LoadedCellReception) and Bonn (LoadedCellReceptionBonn and LLSQC-woDataMerging) with the Loaded Cells on the x-axis and the number of failing s-curves on the y-axis.

CHAPTER 7

Summary and outlook

With the successful integration of the first pre-production LLS the Cell Integration site of Bonn has demonstrated their readiness for the production of the largest ever built silicon pixel detector.

For the Cell Integration site in Bonn to be ready, different testing setups and facilities needed to be built. One of these testing setups is the Loaded Cell QC Box, which was successfully commissioned and validated during this thesis. To adapt the Loaded Cell QC Box to the Cell Integration site in Bonn some modifications were carried out including an easily accessible switch to change between pressurized air and nitrogen for the dry air supply of the box and a structure to enable source scans. For the validation of the box, a digital and standard ITk Pixel module were tested and demonstrating, that the Loaded Cell QC Box is able to perform all of the required tests for the first step of the Cell Integration, the Loaded Cell reception.

With the Loaded Cell QC Box ready for operation an important contribution to the understanding of bump connectivity could be delivered as a bump bond stress test yielded unexpected results and a verification was required. In this test the bump bonds of the ITk Pixel module were tested on their resistance against thermal stress, for which they were thermal cycled in Göttingen. When the first disconnected bumps appeared in the middle of the ITk Pixel module a source scan for confirmation was advised, as disconnected bumps are expected at the edges. The only available test setup for source scans with Loaded Cells in Germany at that time was the Loaded Cell QC Box in Bonn, thanks to the customization made to that box. Therefore the Loaded Cells were sent to Bonn and the source scans performed with the gamma source ^{241}AM. The source scans in Bonn revealed the same disconnected bumps as previously measured in Göttingen verifying the measurements. This lead to the hypothesis that the pick-up/wire bond protection glue points are causing mechanical stress to the ITk Pixel module, which after an excessive amount of thermal cycles results in disconnected bumps. Nevertheless it was concluded, that this is no threat to the ITk, as the disconnected bumps started to show up after 3.5 times the amount of thermal cycles an ITk Pixel module will receive in its lifetime.

In November of 2024 the first pre-production Inclined Half-Ring of the collaboration was ready to be integrated and so was the Cell Integration site Bonn. For this reason a Functional Local Support, two PP0s, several pigtails and 12 Loaded Cells produced in Japan were send to Bonn, to built the first Inclined Half-Ring. Here the Loaded Cell reception was performed in the Loaded Cell QC Box for the 11 Loaded Cells determined for the Half-Ring. The goal of this pre-production was to find issues in the production line and issues in the procedure that could lead to a lesser yield in production. When comparing the results of the Module QC to the Loaded Cell Reception it was found, that the standard procedure results

in no damage to the ITk Pixel module and that the scans performed at both sites yielded similar results. Only one Loaded Cell could not be compared to the Module QC, as the upload of the configurations for that Loaded Cell to the database went wrong and untuned configurations were uploaded. Therefore it is concluded, that the pre-production showed no major problems for the production and only smaller inconveniences like the necessity for pictures in the visual inspection of the Loaded Cell reception and the need for a proper use of the ITk production database arose.

After the successful Loaded Cell reception the pigtail installation and the integration of the Loaded Cells on the Half-Ring could be performed. In the pigtail installation the final production pigtail was glued to the Loaded Cell, in a tool designed specifically for this purpose. This process went well and the only problem that occurred was the bending of the pigtail, which was not optimal and resulted in significant variability in the final shape of the pigtails.

After this the integration of the Loaded Cells to the Half-Ring started. The Half-Ring built is from Layer 3 and with 12 available Loaded Cells only the second PP0 was integrated. In this process the Loaded Cells get screwed to the Base Blocks on the Half-Ring, which are covered with thermal paste. When all of them are integrated on the Half-Ring the PP0 is installed to which the pigtails of each Loaded Cell gets screwed with an interposer in between to guarantee the electrical connection. Here it was found, that the installation of these interposers is quite difficult at the periphery of the Half-Ring. In the following electrical test it was than revealed, that during installation the last three interposers got damaged and bend teeth lead to a connection of the LV power to ground. Thanks to the design accounting for re-workability, it was possible to fix the error. In the end the full electrical tests were performed by A. Wald and showed that the first Cell Integration worked well and no Loaded Cell was damaged in the procedure. With all of this the pre-production can be concluded as a success and only minor issues needed to be fixed.

An outlook for the Loaded Cell QC Box is a better adaption to the production cycle with automated procedures and programs, which can result from the knowledge of the pre-production. Furthermore new Loaded Local Supports are build in the whole collaboration and more will be send to Bonn in the coming year, for which some last preparations need to made. For the successfully integrated Half-Ring the journey went on to the University of Geneva, where it will be thermal cycled and further tested. Afterwards it shall be send to other Cell Integration sites for them to test it and gain experience with the procedures that have been successfully executed in Bonn.

APPENDIX A

Appendix - Source scans on ITk Pixel modules for a bump bond stress test

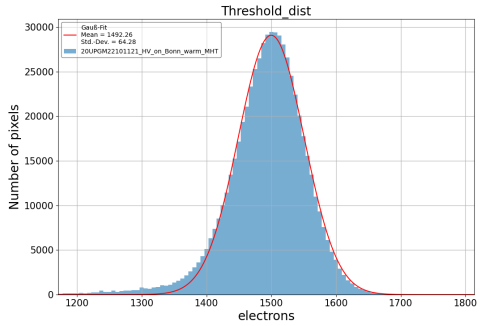
In the following the digital, analog, threshold and disconnected bump data for the three Loaded Cell, 121, 122, 123 and 124, missing in the main part are displayed.

Loaded Cell	$\frac{\text{Occupancy}}{\text{Injections}}$	Masked	Failing
121	614106	294	0
122	614290	110	0
123	614161	239	0
124	614400	0	0

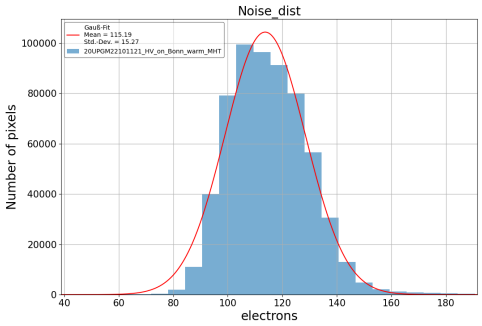
Table A.1: Data of the digital scan for the different Loaded Cells from the bump bond stress test tested with 100 injections

Loaded Cell	$\frac{\text{Occupancy}}{\text{Injections}}$	Masked	Failing
121	614077.20	294	33
122	614265.75	110	26
123	614215.31	0	205
124	614356.80	0	54

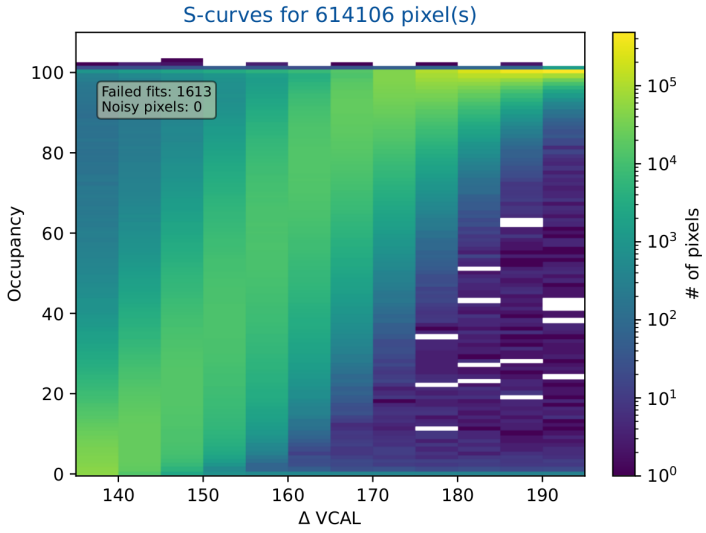
Table A.2: Data of the analog scan for the different Loaded Cells from the bump bond stress test tested with 100 injections



Threshold distribution

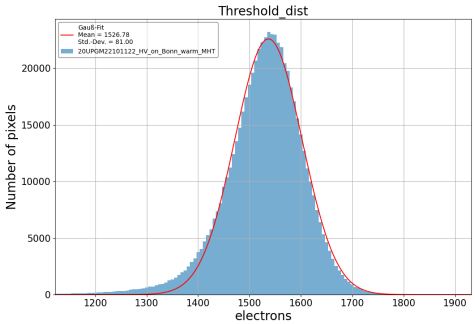


Noise distribution

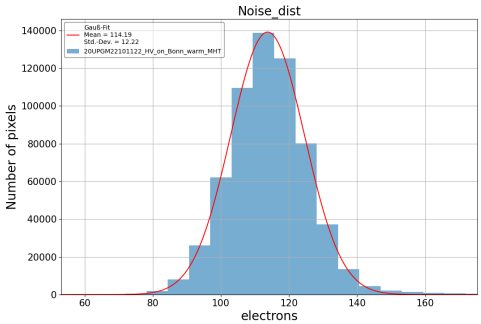


S-curves

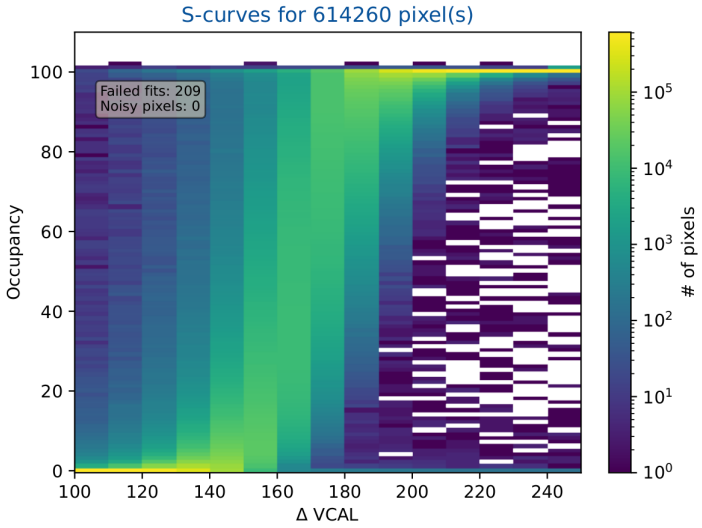
Figure A.1: Threshold scan of Loaded Cell 121 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution

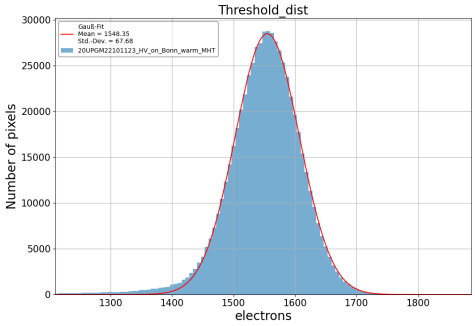


Noise distribution

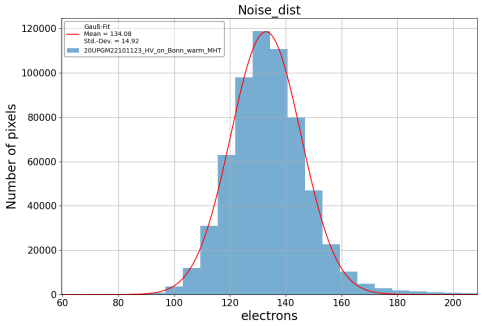


S-curves

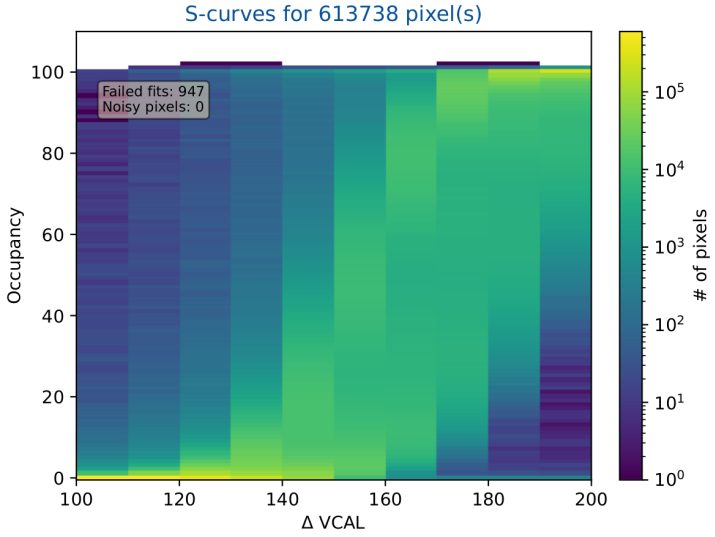
Figure A.2: Threshold scan of Loaded Cell 122 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution

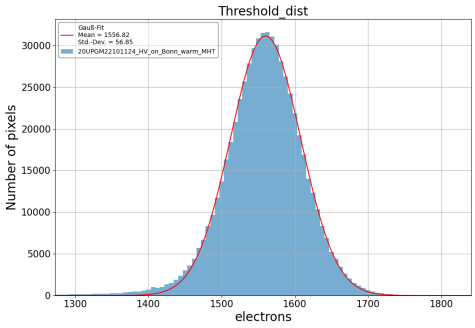


Noise distribution

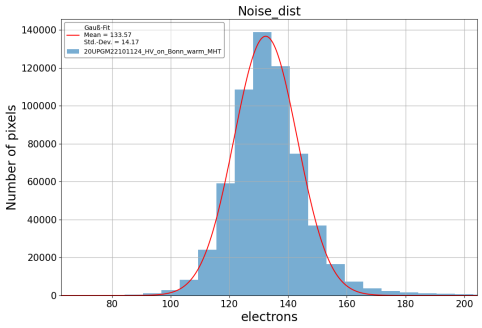


S-curves

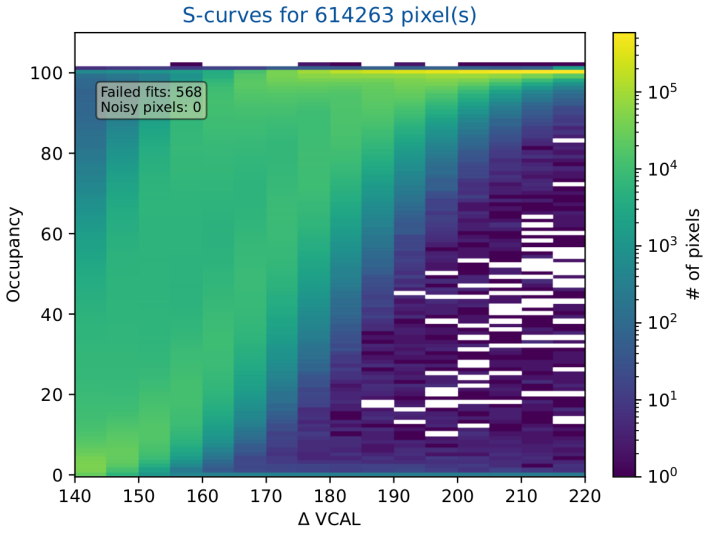
Figure A.3: Threshold scan of Loaded Cell 123 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution

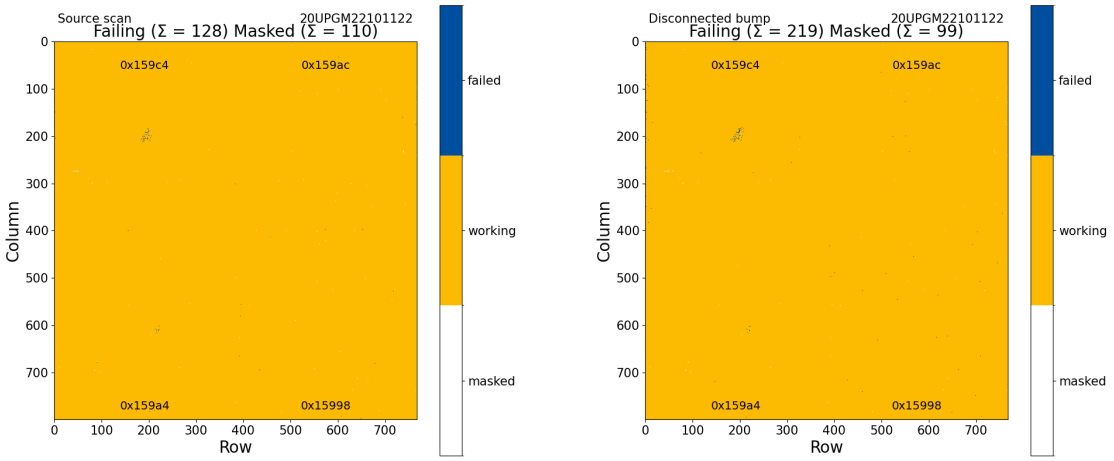


Noise distribution



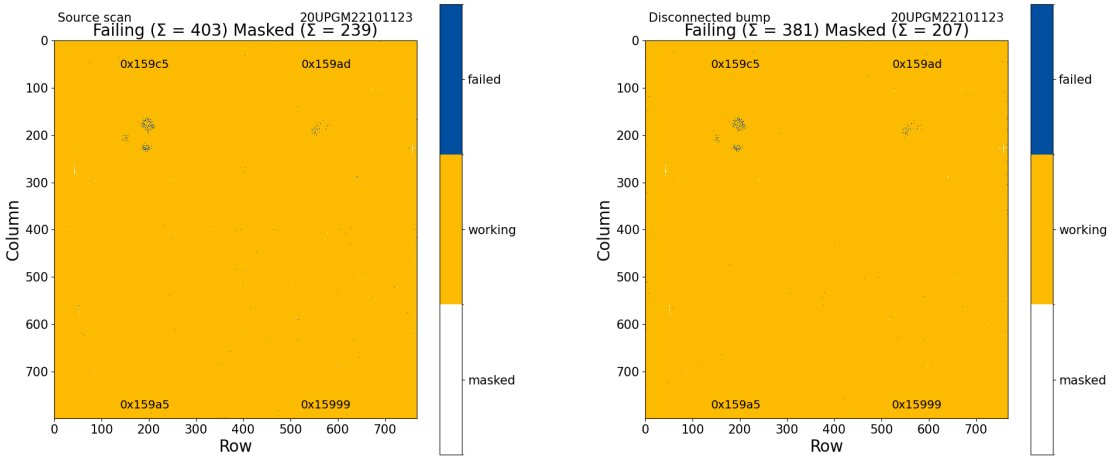
S-curves

Figure A.4: Threshold scan of Loaded Cell 124 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



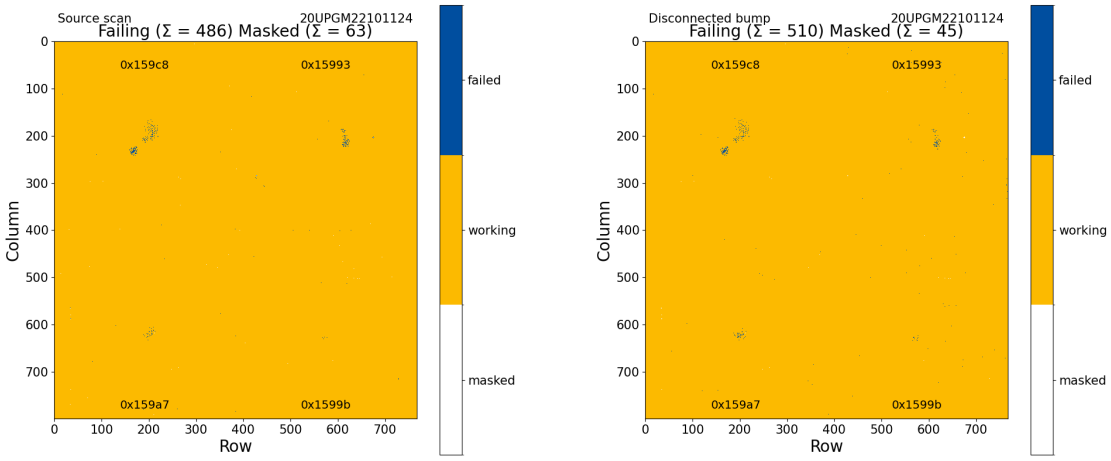
(a) (b)

Figure A.5: Disconnected bump maps from Bonn (a) and Göttingen (b) for module 122, with the same pattern of disconnected bumps.



(a) (b)

Figure A.6: Disconnected bump maps from Bonn (a) and Göttingen (b) for module 123, with the same pattern of disconnected bumps.



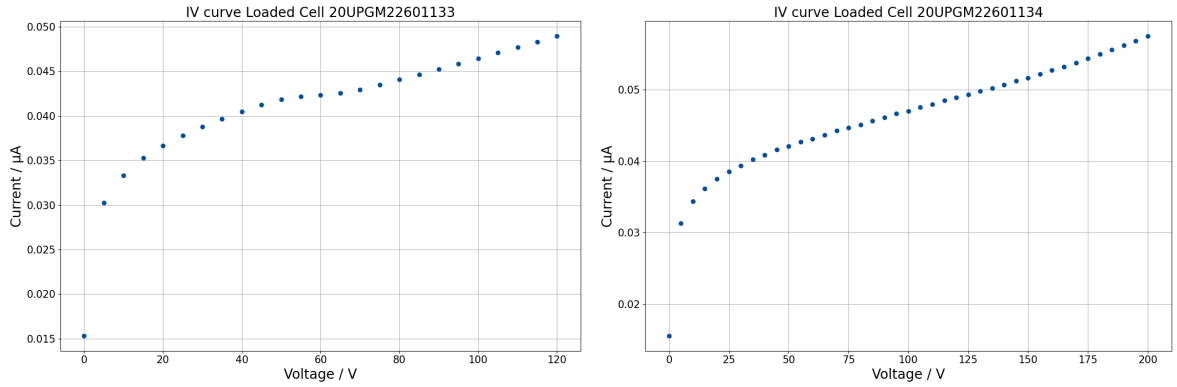
(a) (b)

Figure A.7: Disconnected bump maps from Bonn (a) and Göttingen (b) for module 124, with the same pattern of disconnected bumps.

APPENDIX B

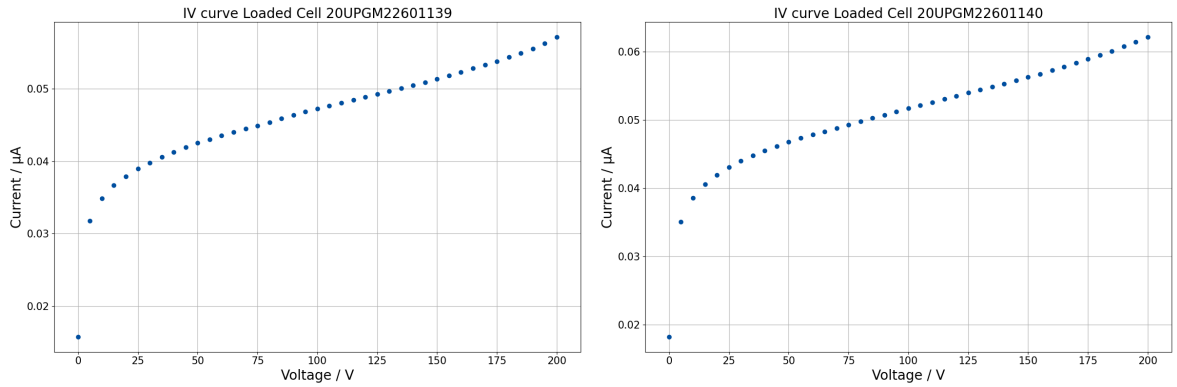
Appendix - First pre-production Half-Ring

In the following the missing IV curves of the Loaded Cells, tables with the data of the different scans of the PFA made in Bonn, the threshold scan data and the self trigger source scans are shown.



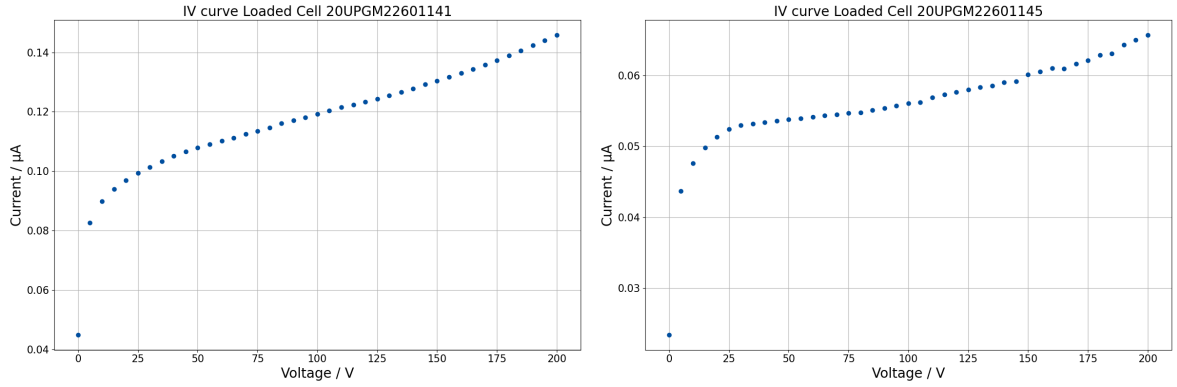
(a) (b)

Figure B.1: IV curves from the sensor of the Loaded Cell 133 and 134 supplied with a voltage up to 200 V measured in 5 V steps.



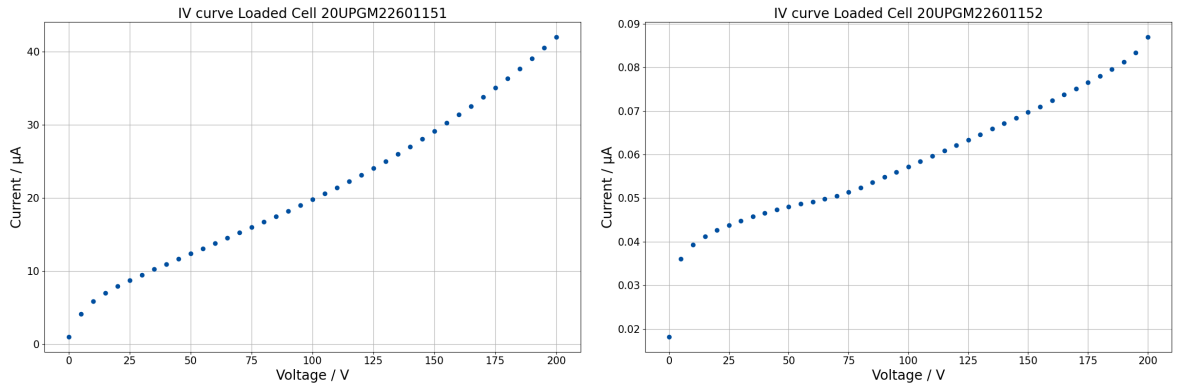
(a) (b)

Figure B.2: IV curves from the sensor of the Loaded Cell 139 and 140 supplied with a voltage up to 200 V measured in 5 V steps.



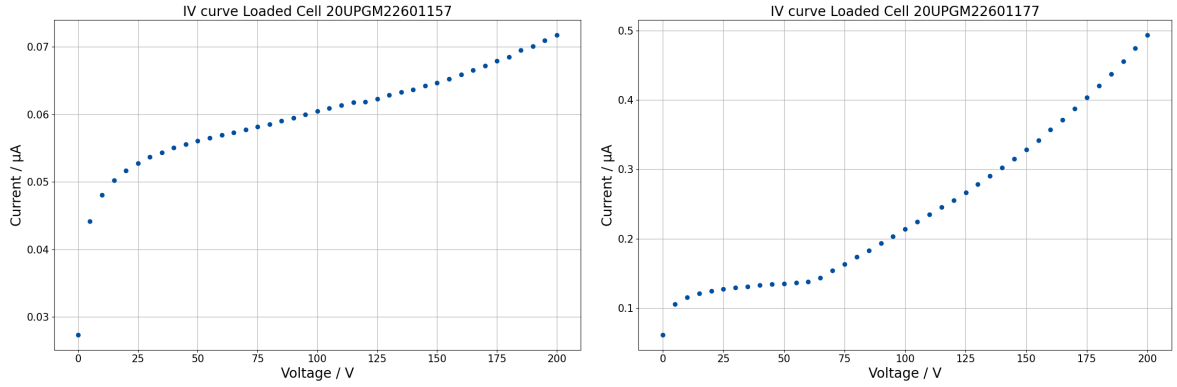
(a) (b)

Figure B.3: IV curves from the sensor of the Loaded Cell 141 and 145 supplied with a voltage up to 200 V measured in 5 V steps.



(a) (b)

Figure B.4: IV curves from the sensor of the Loaded Cell 151 and 152 supplied with a voltage up to 200 V measured in 5 V steps.



(a) (b)

Figure B.5: IV curves from the sensor of the Loaded Cell 157 and 177 supplied with a voltage up to 200 V measured in 5 V steps.

Loaded Cell	$\frac{\text{Occupancy}}{\text{Injections}}$	Masked	Failing
095	613632	768	0
133	614344	0	56
134	611184	3216	0
139	614400	0	0
140	614400	0	0
141	611328	3072	0
145	614400	0	0
151	614403	0	3
152	614399	0	1
157	614395.12	0	12
177	611322	3072	6

Table B.1: Data of the digital scan for the different Loaded Cells tested with 100 injections

Loaded Cell	$\frac{\text{Occupancy}}{\text{Injections}}$	Masked	Failing
095	613601.89	768	44
133	614320.30	0	89
134	611175.11	3216	9
139	614341.48	0	67
140	614371.26	0	42
141	611258.01	3072	87
145	614365.06	0	52
151	614346.87	0	82
152	459269.86	0	155176
157	614344.20	0	81
177	611237.39	3072	119

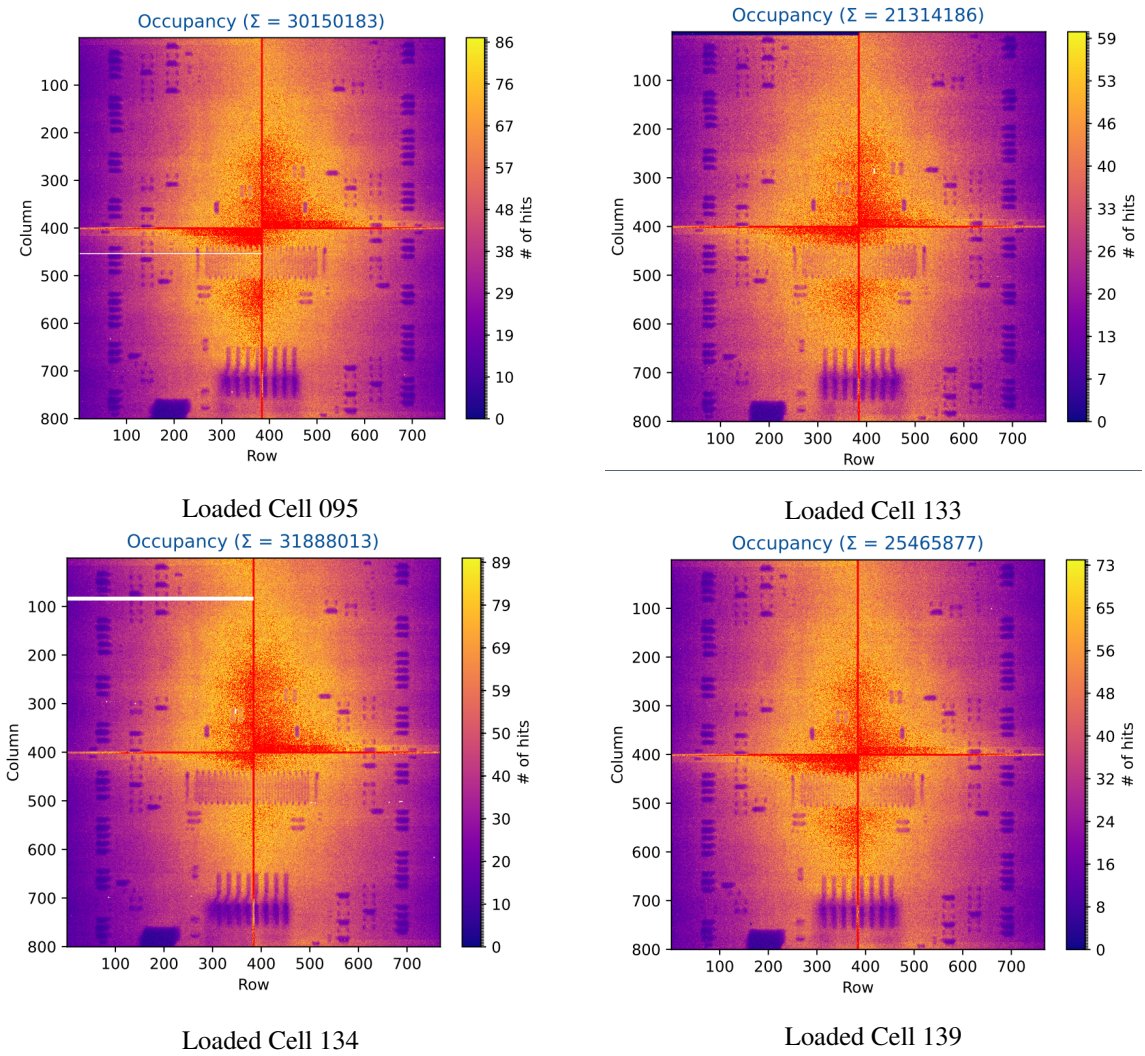
Table B.2: Data of the analog scan for the different Loaded Cells tested with 100 injections

Loaded Cell	Occupancy	Masked	Failing
095	130	833	1
133	913	101	9
134	323	3216	3
139	780	0	6
140	233	91	1
141	3621	3072	32
145	884	0	4
151	295	108	3
152	639	0	1
157	1911	0	15
177	5776	3072	49

Table B.3: Data of the merged bump scan for the different Loaded Cells tested with 100 injections in the surrounding pixels

Loaded Cell	Occupancy	Masked	Failing
095	30150183	833	37
133	21314186	43	1861
134	31888013	3216	50
139	25465877	65	115
140	28476205	91	192
141	31421566	3163	31
145	29522898	62	48
151	33160792	108	71
152	19110618	192	1512
157	29994756	84	64
177	-	-	-

Table B.4: Data of the disconnected bump scan for the different Loaded Cells tested with a ^{241}Am source



Loaded Cell 095

Loaded Cell 133

Loaded Cell 134

Loaded Cell 139

Figure B.6: Self trigger source scans of 6 Loaded Cells prepared for the Half-Ring illuminated for one hours with ^{241}AM.

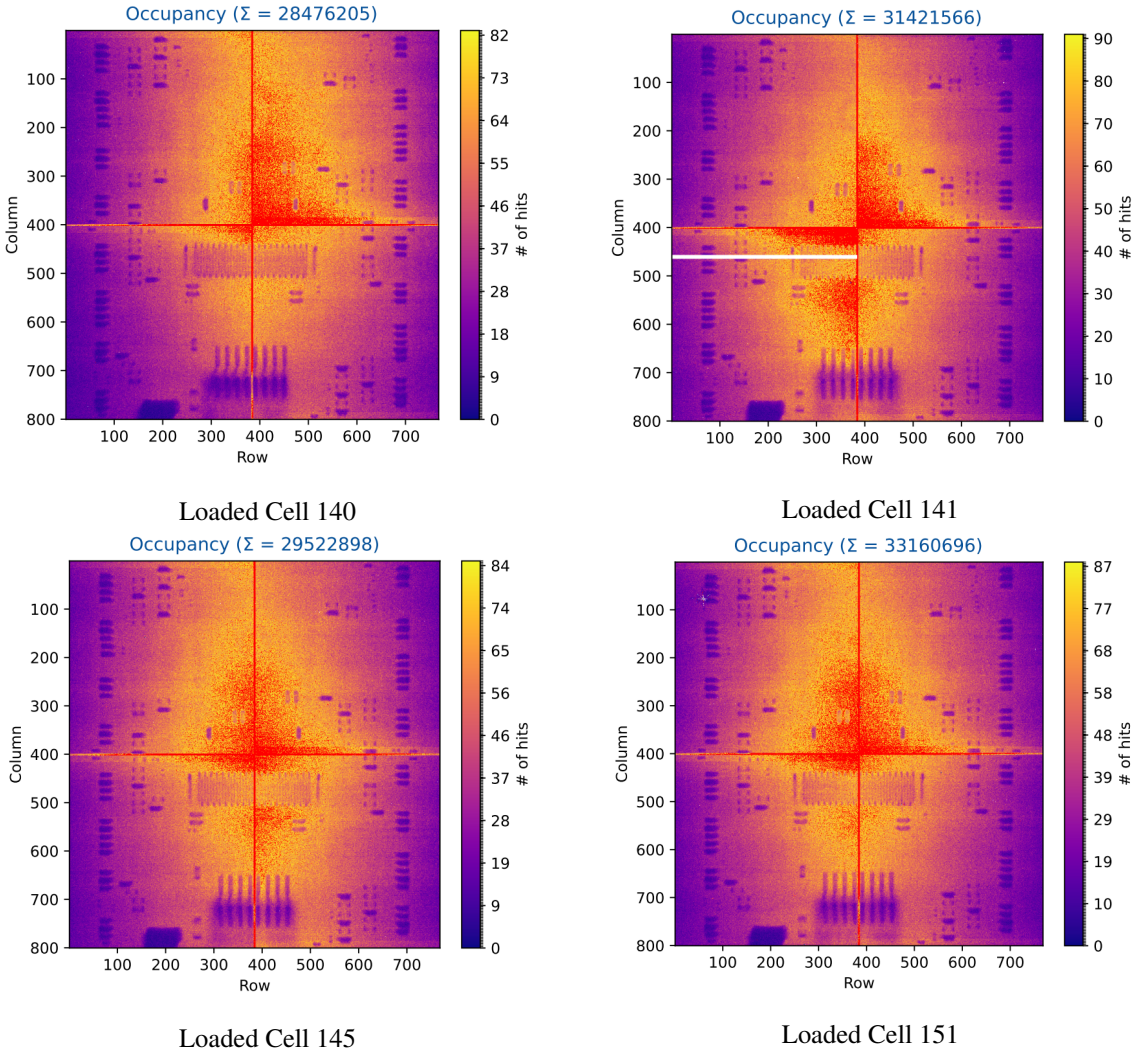
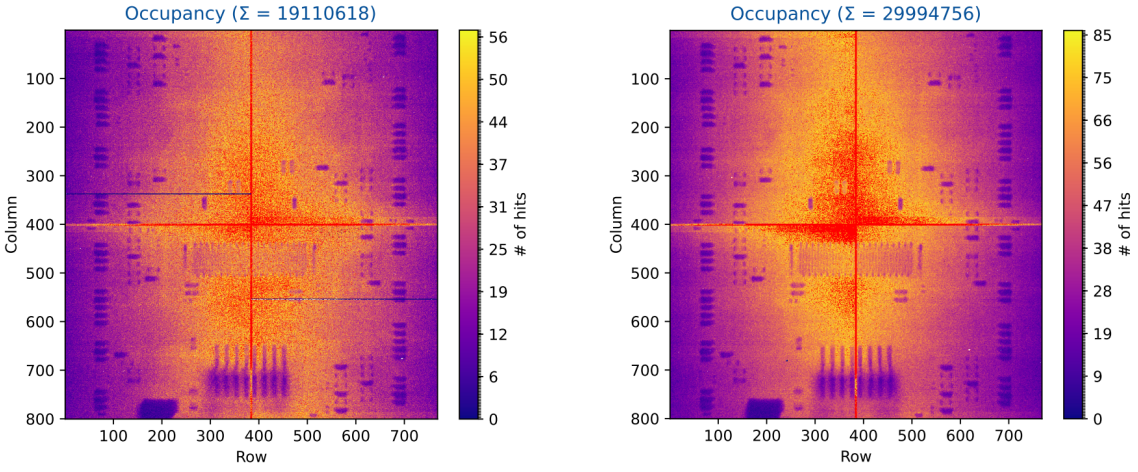
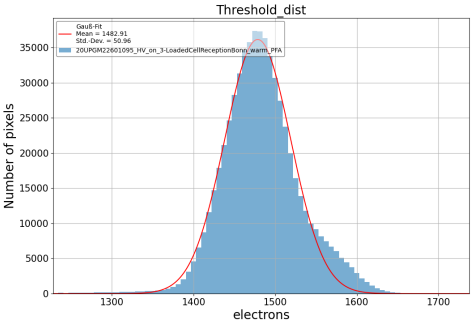


Figure B.7: Self trigger source scans of 4 Loaded Cells prepared for the Half-Ring illuminated for one hours with ^{241}AM.

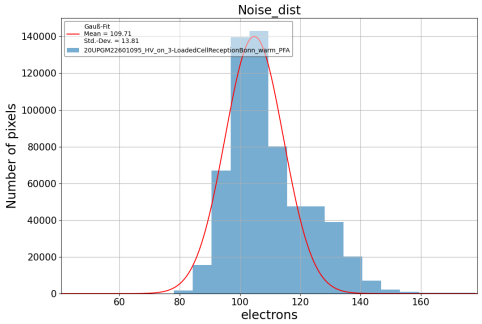


Loaded Cell 152 Loaded Cell 157

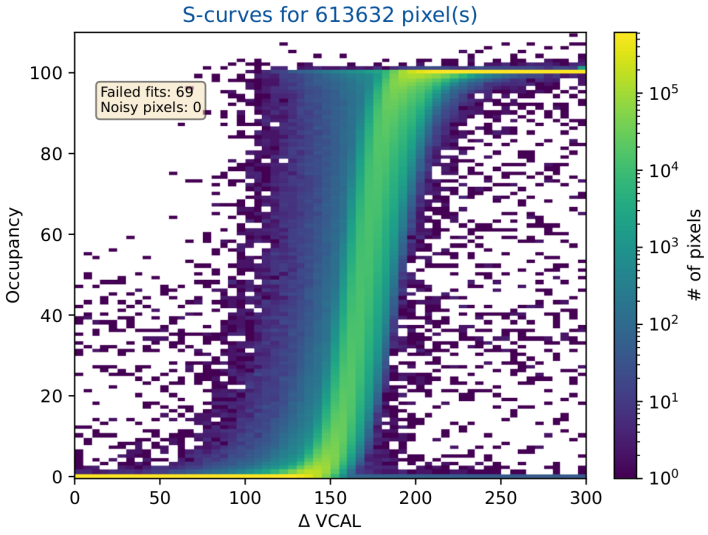
Figure B.8: Self trigger source scans of 2 Loaded Cells prepared for the Half-Ring illuminated for one hours with ^{241}AM.



Threshold distribution

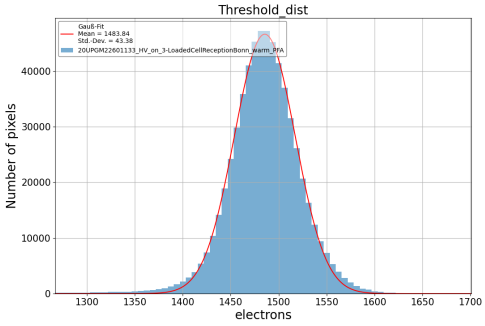


Noise distribution

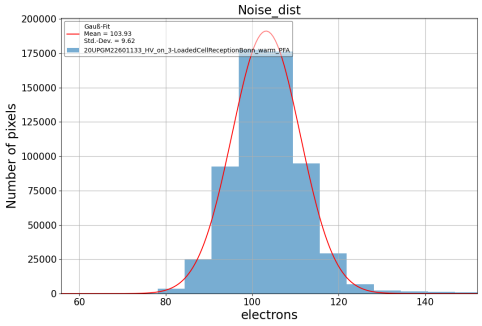


S-curves

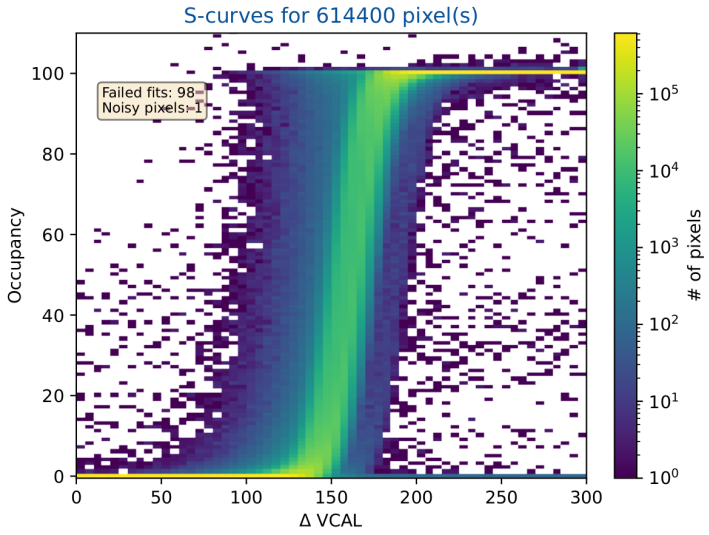
Figure B.9: Threshold scan of Loaded Cell 095 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution

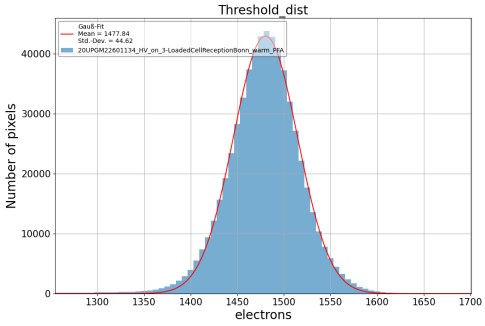


Noise distribution

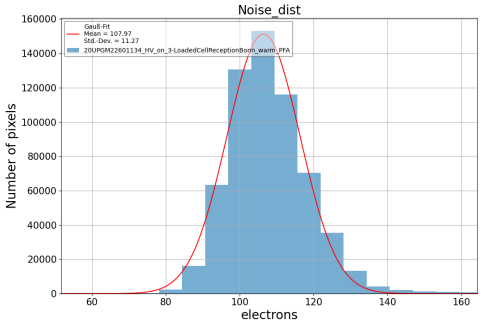


S-curves

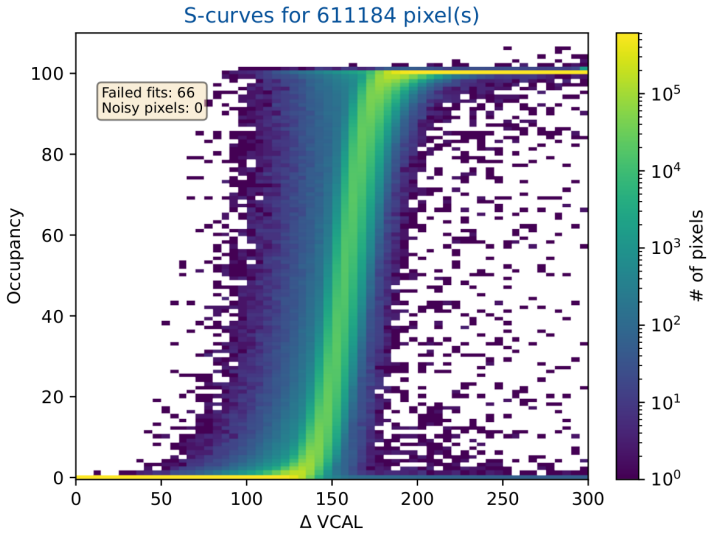
Figure B.10: Threshold scan of Loaded Cell 133 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution

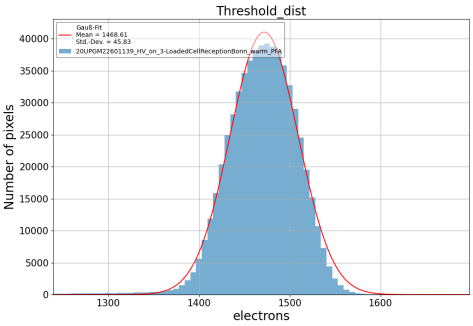


Noise distribution

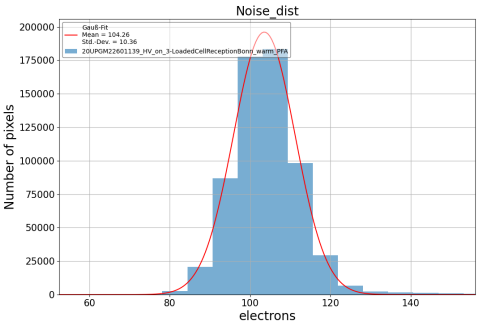


S-curves

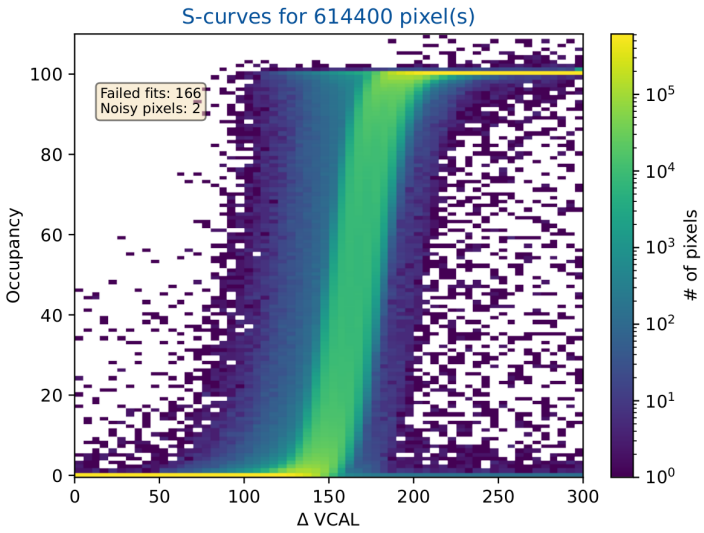
Figure B.11: Threshold scan of Loaded Cell 134 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution

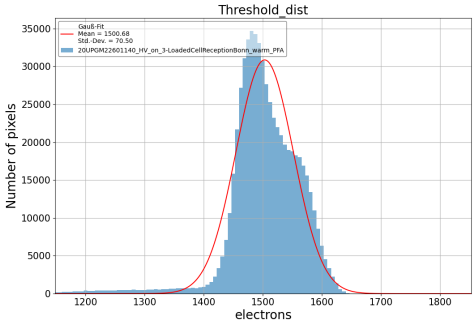


Noise distribution

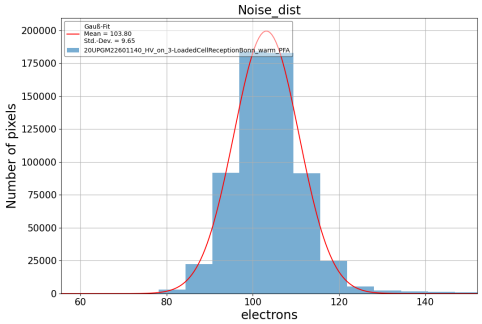


S-curves

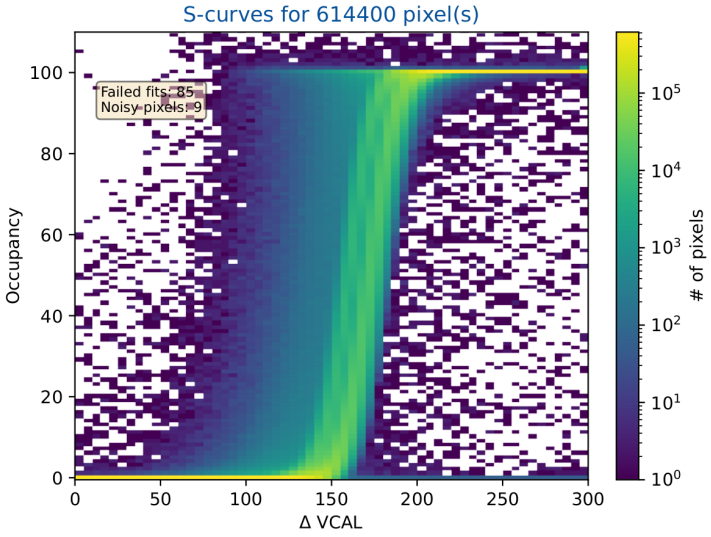
Figure B.12: Threshold scan of Loaded Cell 139 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution

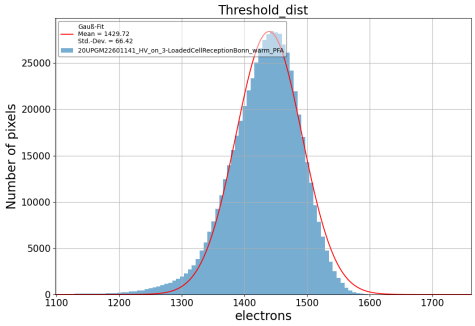


Noise distribution

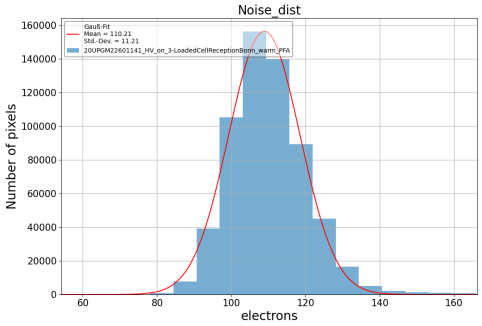


S-curves

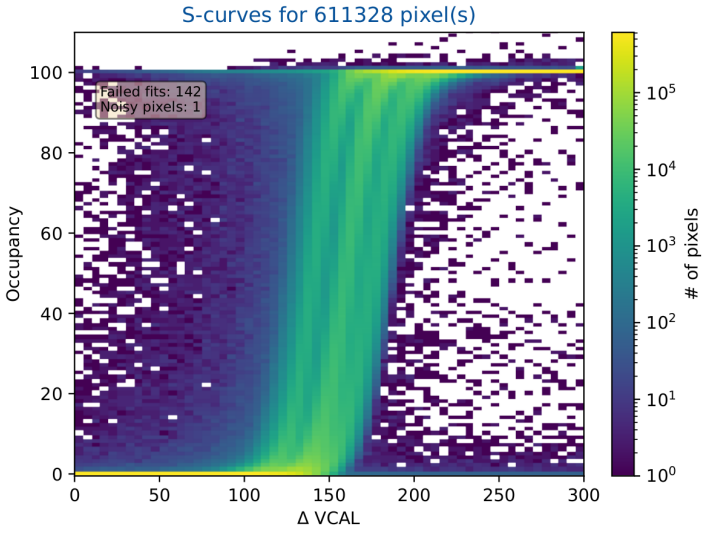
Figure B.13: Threshold scan of Loaded Cell 140 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution

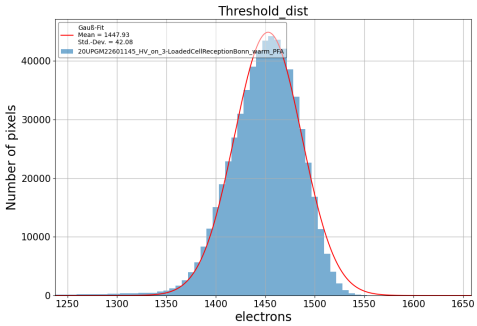


Noise distribution

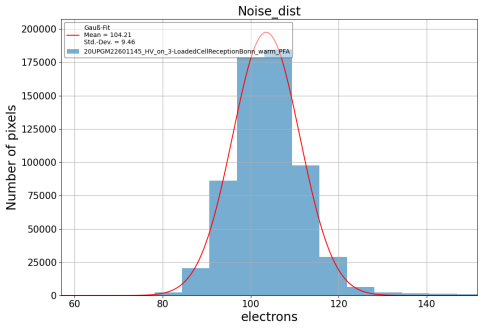


S-curves

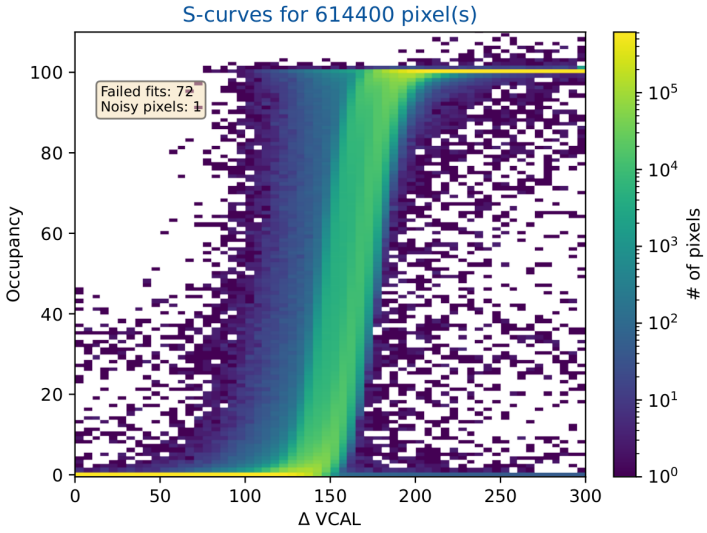
Figure B.14: Threshold scan of Loaded Cell 141 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution

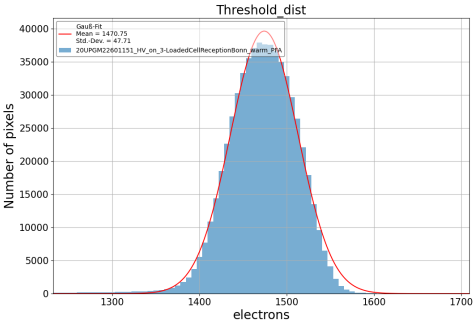


Noise distribution

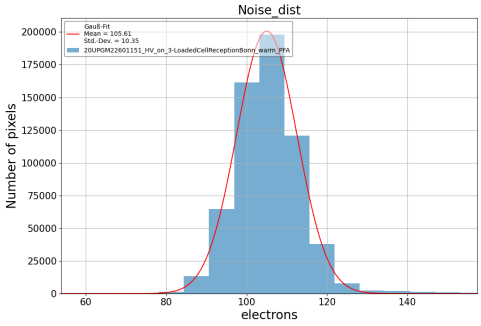


S-curves

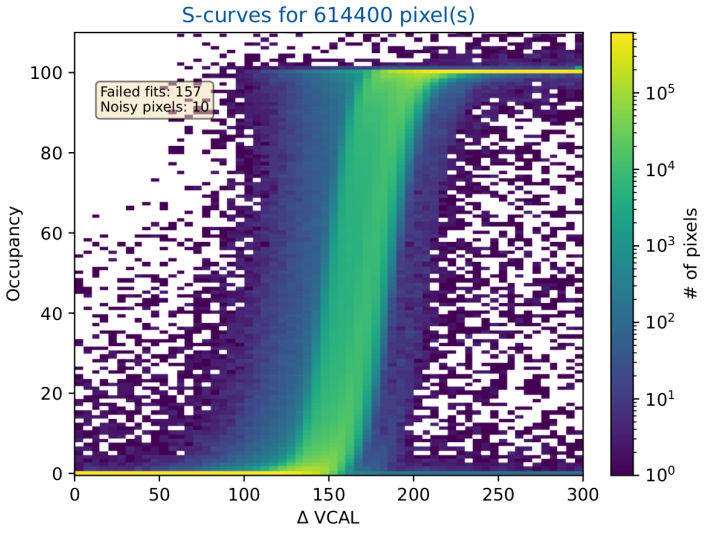
Figure B.15: Threshold scan of Loaded Cell 145 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution

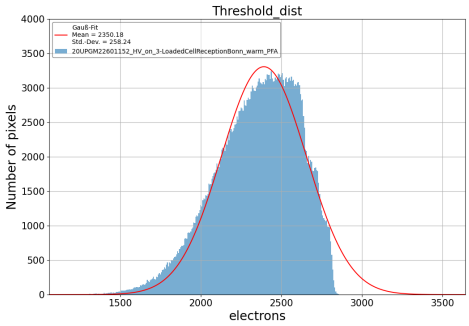


Noise distribution

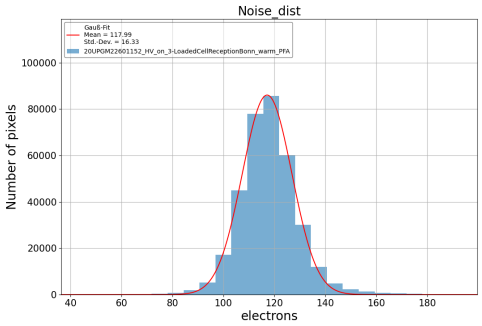


S-curves

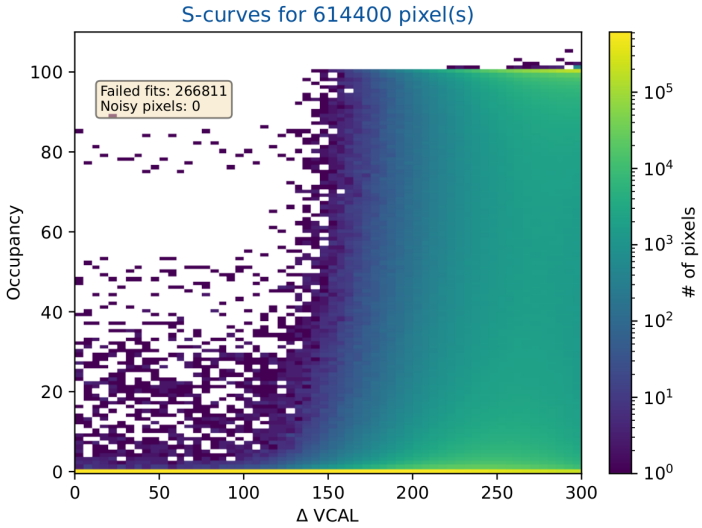
Figure B.16: Threshold scan of Loaded Cell 151 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution

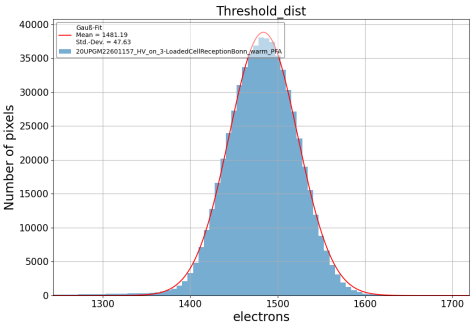


Noise distribution

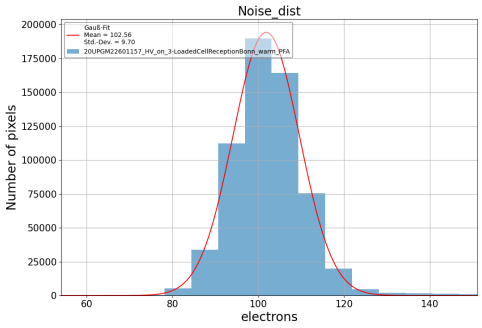


S-curves

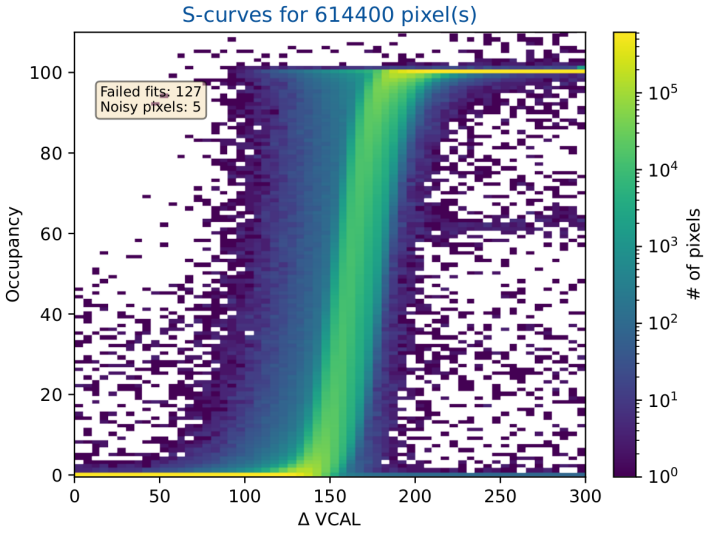
Figure B.17: Threshold scan of Loaded Cell 152 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution

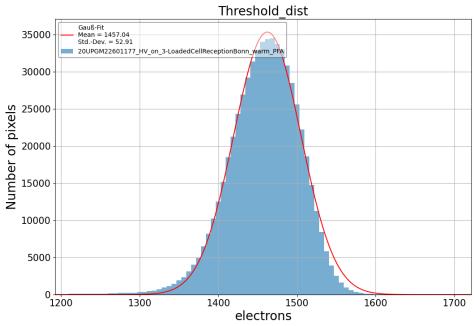


Noise distribution

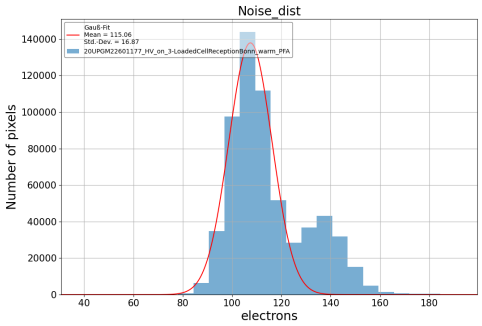


S-curves

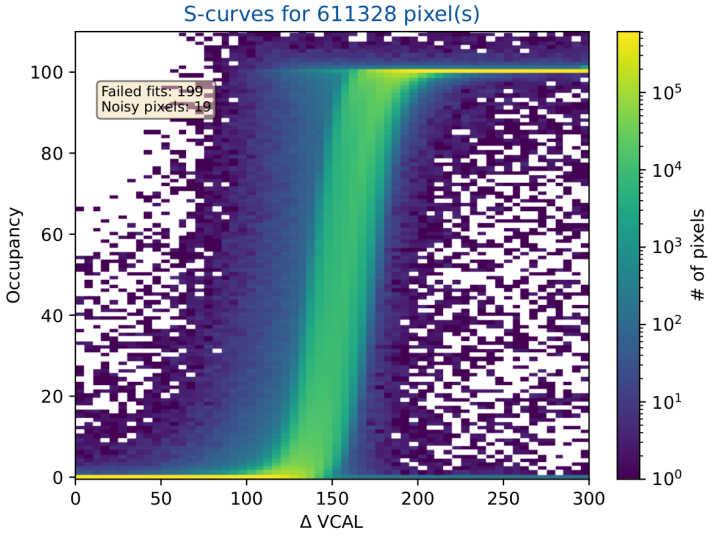
Figure B.18: Threshold scan of Loaded Cell 157 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.



Threshold distribution



Noise distribution



S-curves

Figure B.19: Threshold scan of Loaded Cell 177 including the gauss-fit to the threshold and noise distribution and the s-curves with the failed fits.

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