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FIRMWARE DEVELOPMENT FOR THE SCALABLE READOUT SYSTEM (SRS) WITH VMM3A

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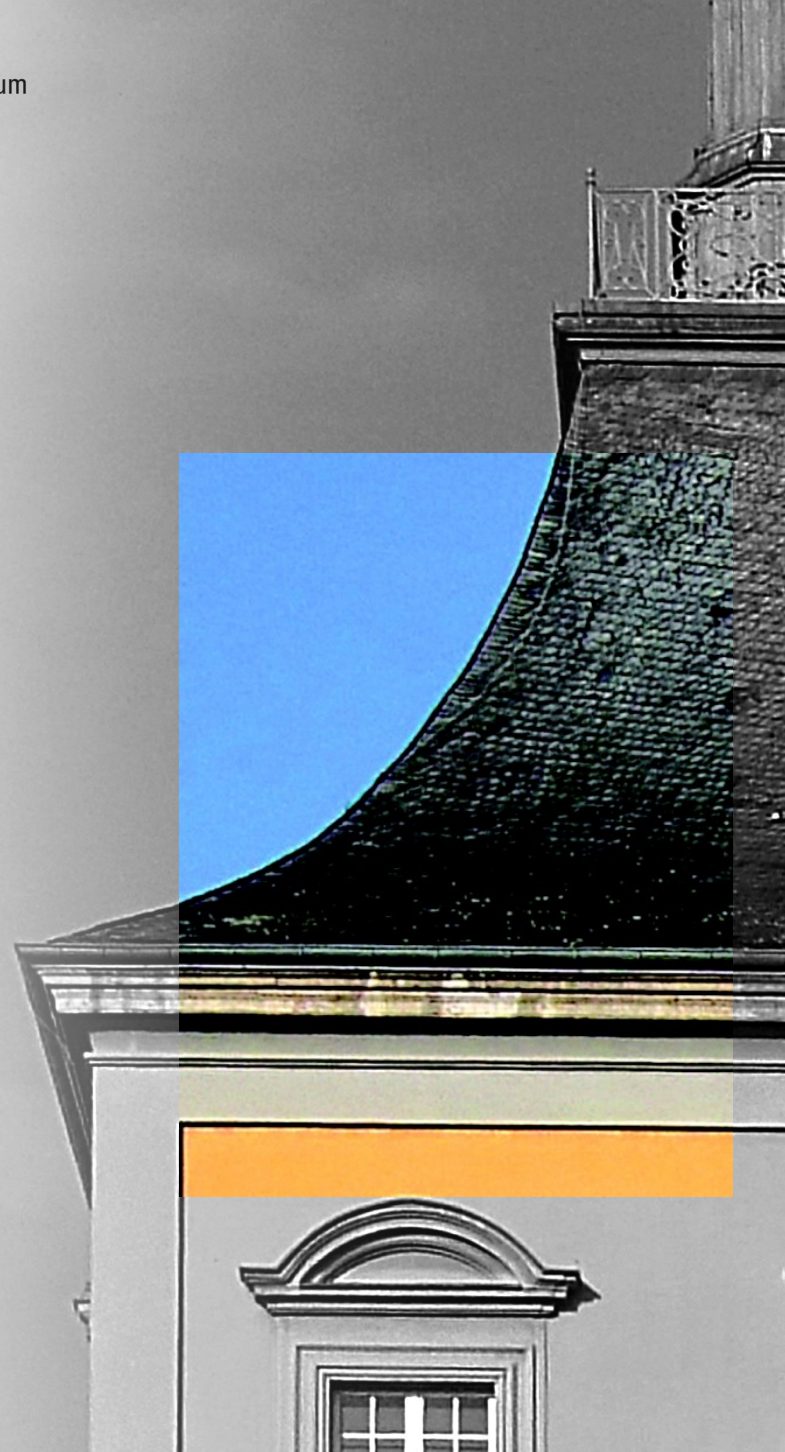

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OUTLINE

- The Scalable Readout System
- The VMM ASIC

- VMM readout
- New hybrid firmware
- Reduced VMM data rate
- Firmware data rate comparison
- Summary

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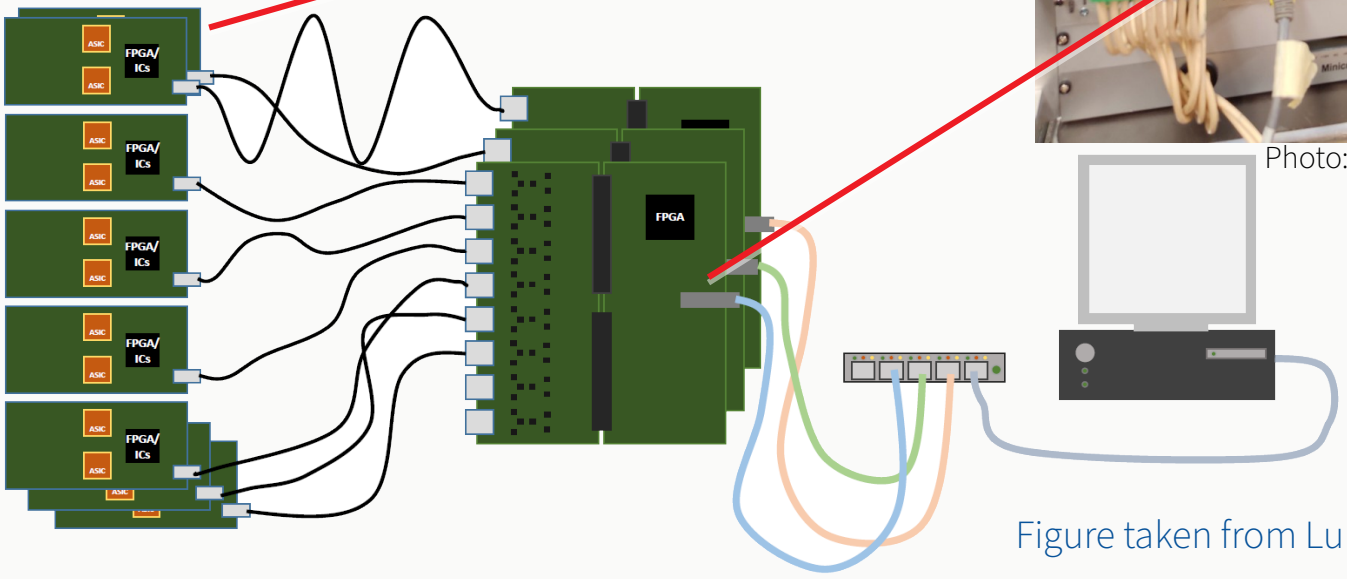
SCALABLE READOUT SYSTEM

- Versatile read-out system (Muller et al., 2013)
- Scalable from a few dozen to many thousand channels
- Compatible with different front-end ASICs
- Implemented: e.g. Timepix3, APV25 and VMM

Related: T 20.6

Structure of the SRS:



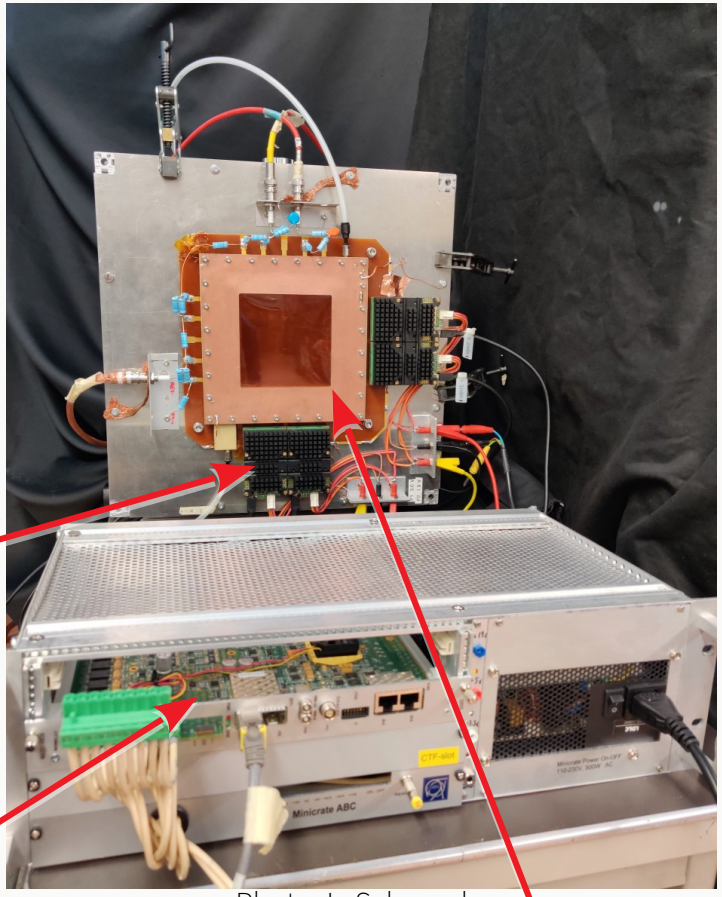


Photo: L. Scharenberg

Triple-GEM detector

Figure taken from Lupberger et al., 2018

Hybrid → HDMI cable → Adapter card + FEC → Ethernet → Switch →Ethernet → PC

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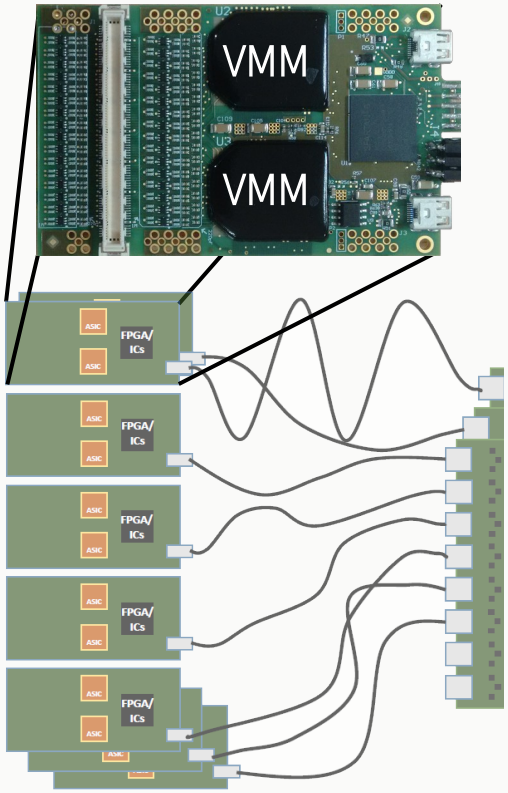
THE VMM

- Front-end ASIC for tracking detectors (De Geronimo et al., 2012)
- Current version: VMM3a (Bakalis, C., 2019)
- Highly flexible, large range of configuration parameters
- Continuous readout at high rates, low electronic noise
- 64 channels per VMM → 128 channels per Hybrid
- Each channel can handle up to 4 MHits/s

VMM used in e.g.:

- ATLAS New Small Wheel (Micromegas and sTGC detectors)
- NMX instrument at ESS in Lund, Sweden

→ SRS combined with VMM very flexible setup



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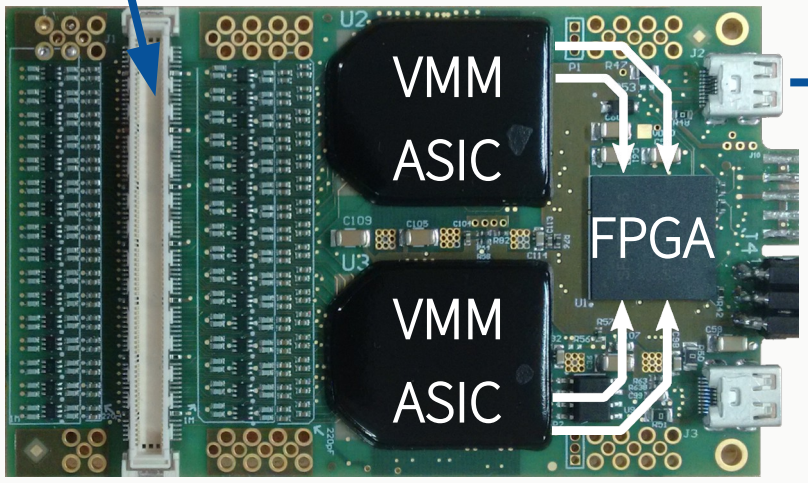
DATA TRANSFER BETWEEN VMM AND FPGA

- VMM reads and digitises analog data directly from detector
- Generates 38 bits of data per hit (timing, amplitude etc.)
- Two data links per VMM to FPGA
- VMM: Up to 200 MHz DDR (Double Data Rate) supported
- FPGA: Previous firmware 160 MHz DDR supported
- 200 MHz DDR would allow 800 Mb/s data transfer

  → Would correspond to 21 MHits/s

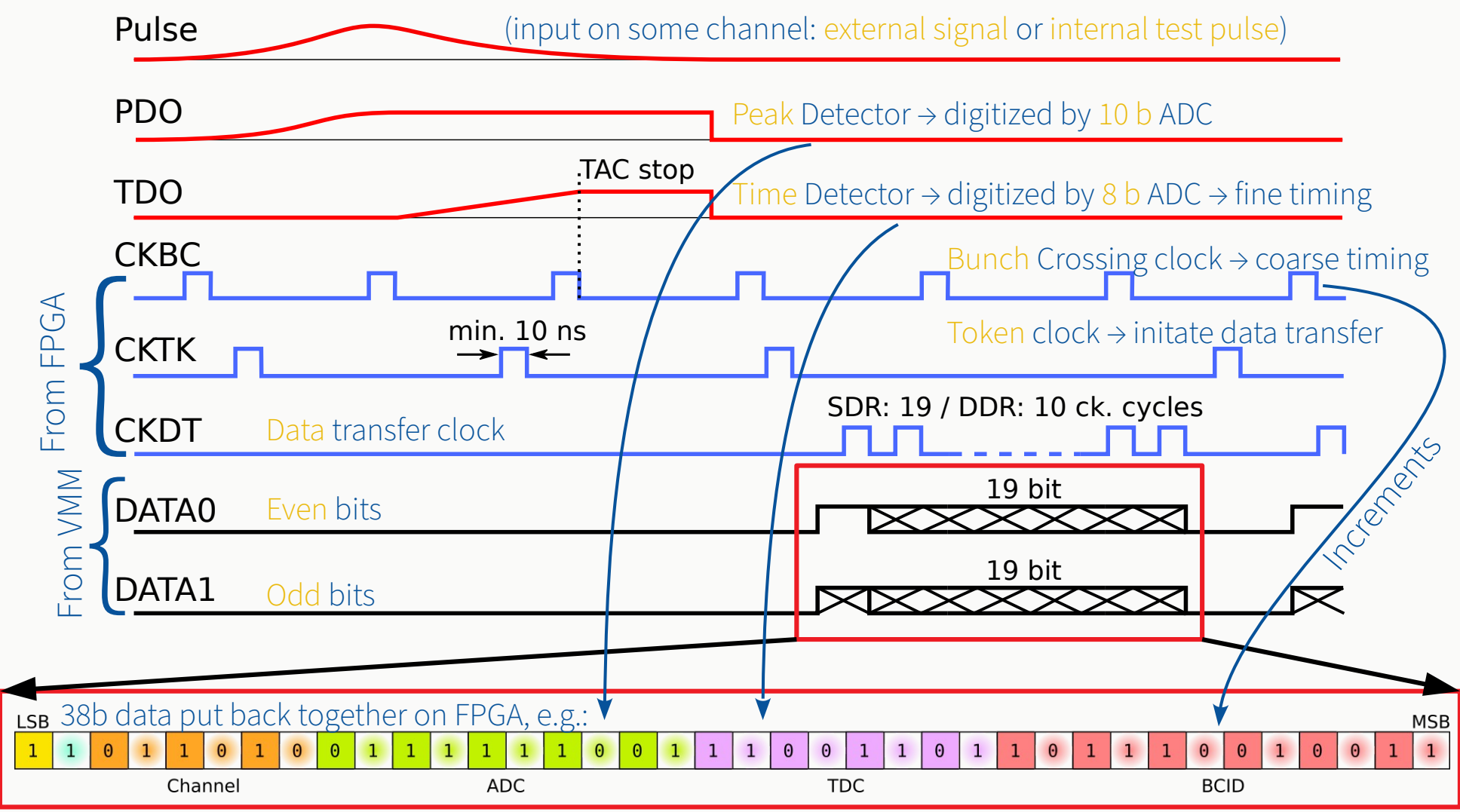
  → Finite amount of storage in VMM: Fetch data as quickly as possible

Plugged onto detector



HDMI to Adapter card

DATA TRANSFER BETWEEN VMM AND FPGA



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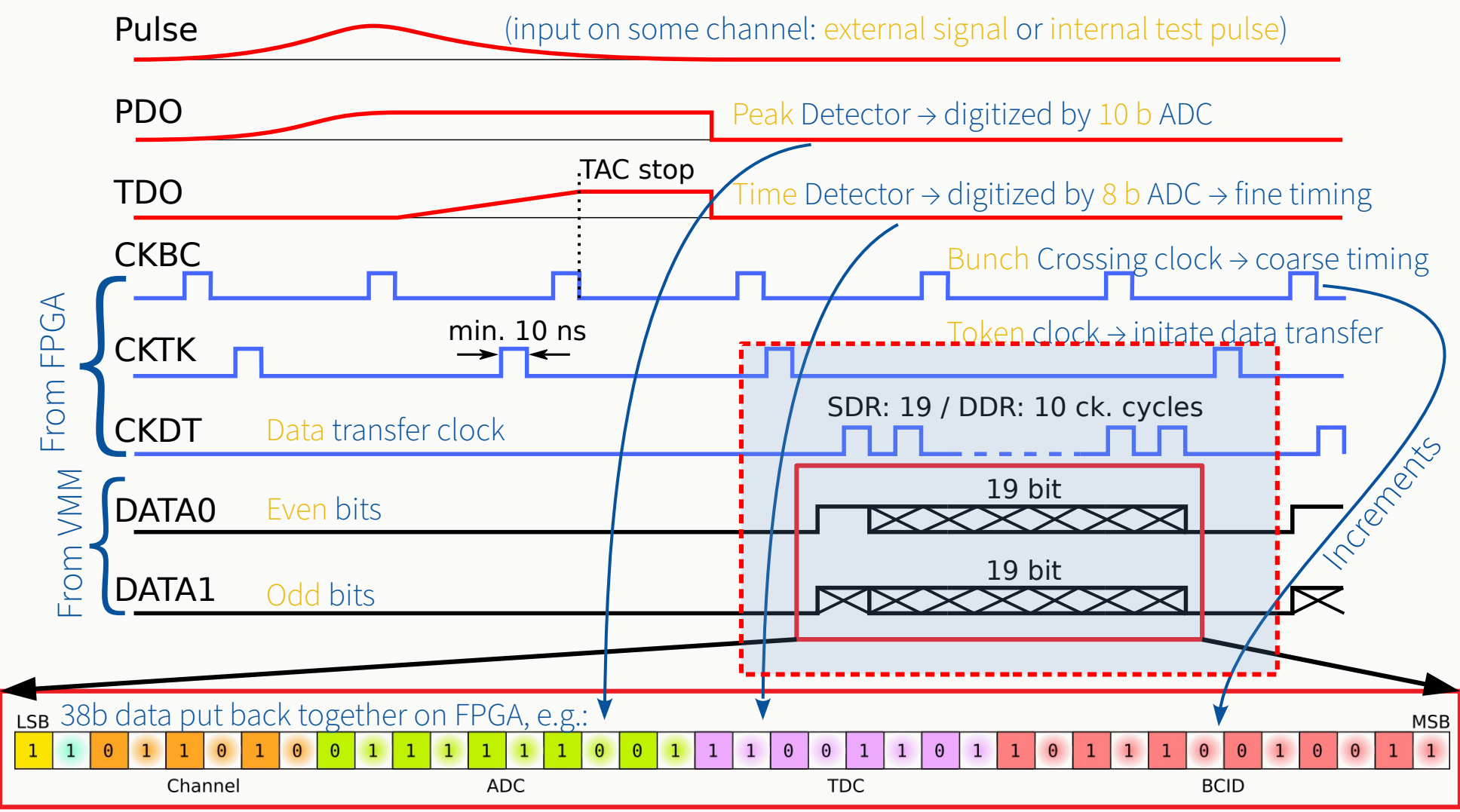
DATA TRANSFER BETWEEN VMM AND FPGA



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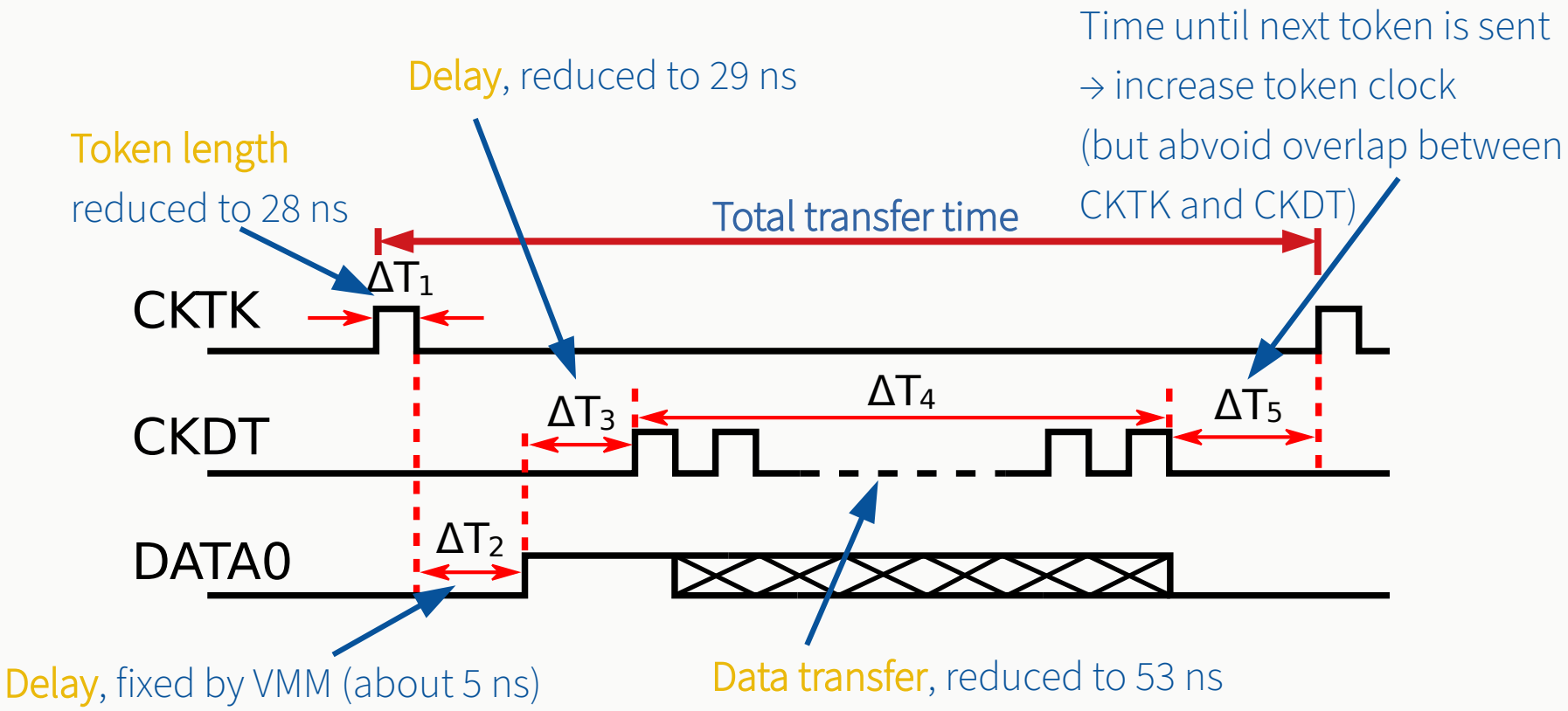
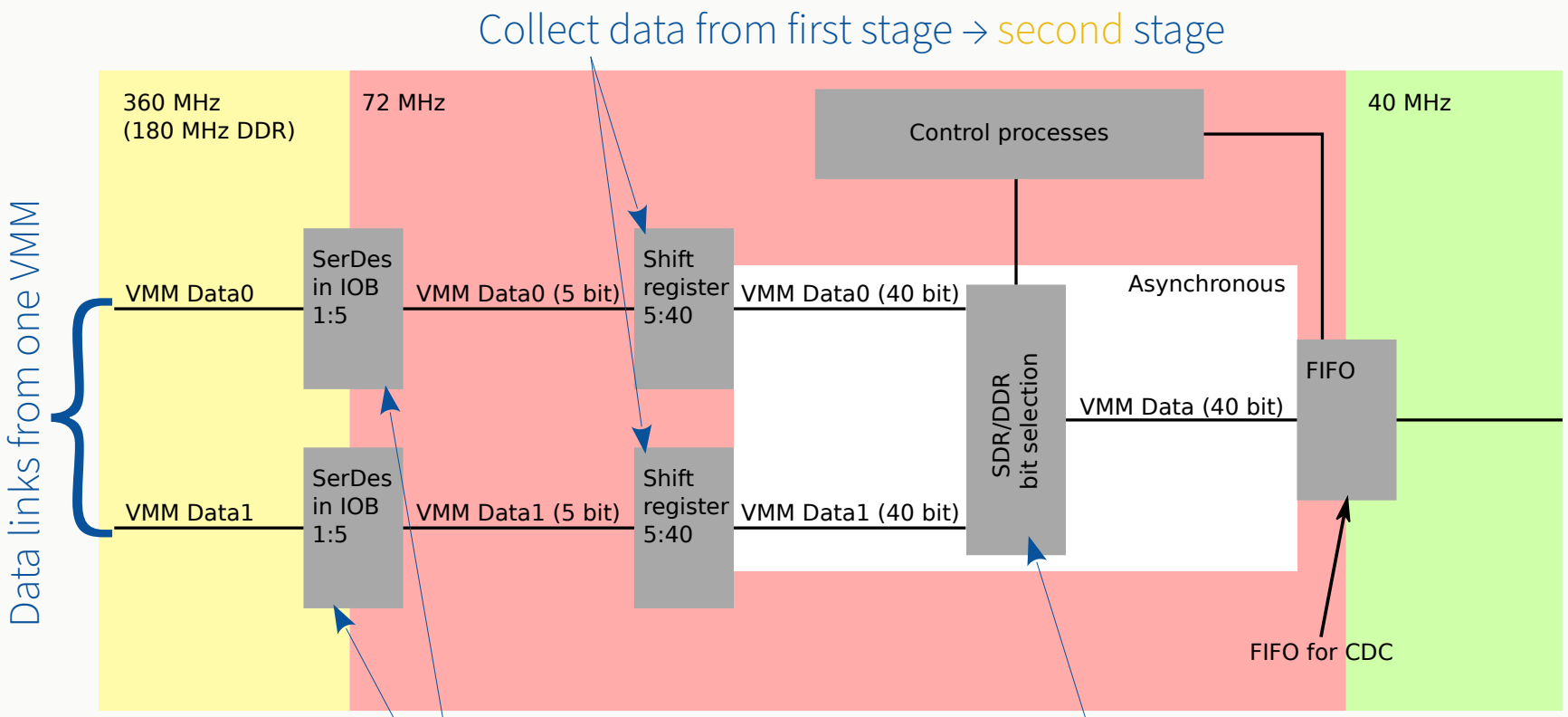
TIME SEGMENTS OF SINGLE DATA TRANSFER



- Old firmware version: 300 ns per complete data transfer
- For new firmware: Transfer time of 125 ns → ideal, equal to HDMI transfer time
- Solution in form of two-stage data deserialiser

STRUCTURE OF THE DATA DESERIALISER



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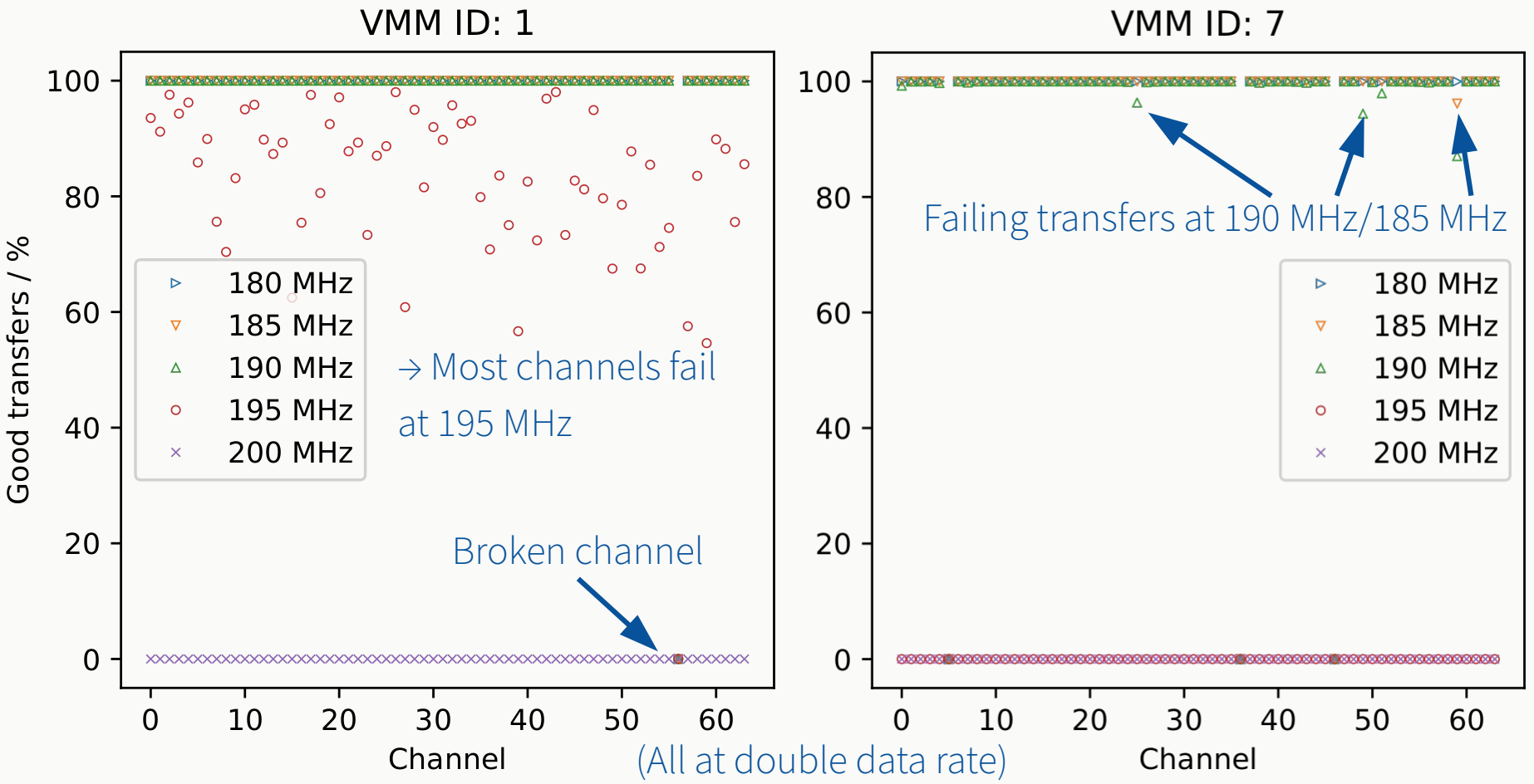
MAXIMUM VMM DATA CLOCK

Two examples of tested devices:



(All at double data rate)

Data transfers with readout clock > 180 MHz DDR unstable

No VMM with stable 200 MHz DDR data transfer

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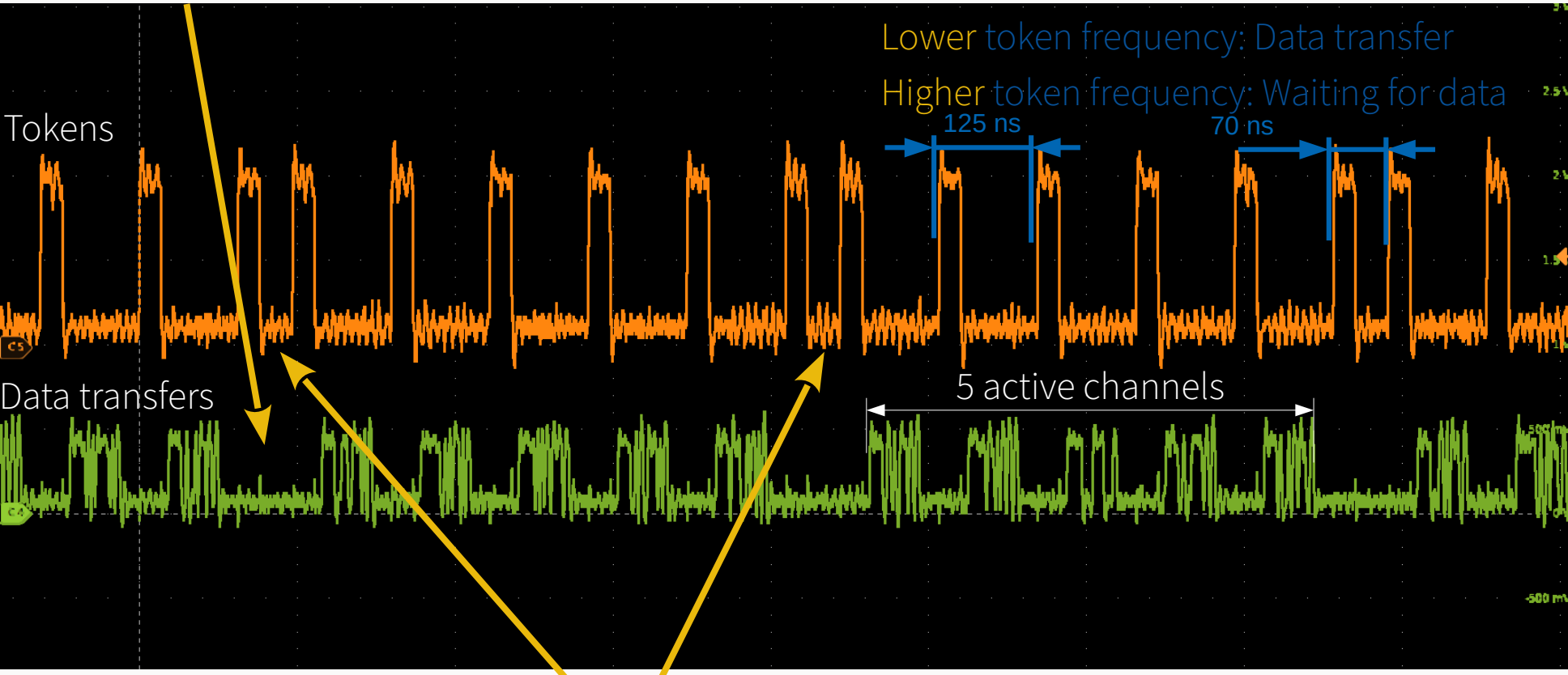
REDUCED DATA RATE DUE TO EXTRA TOKEN

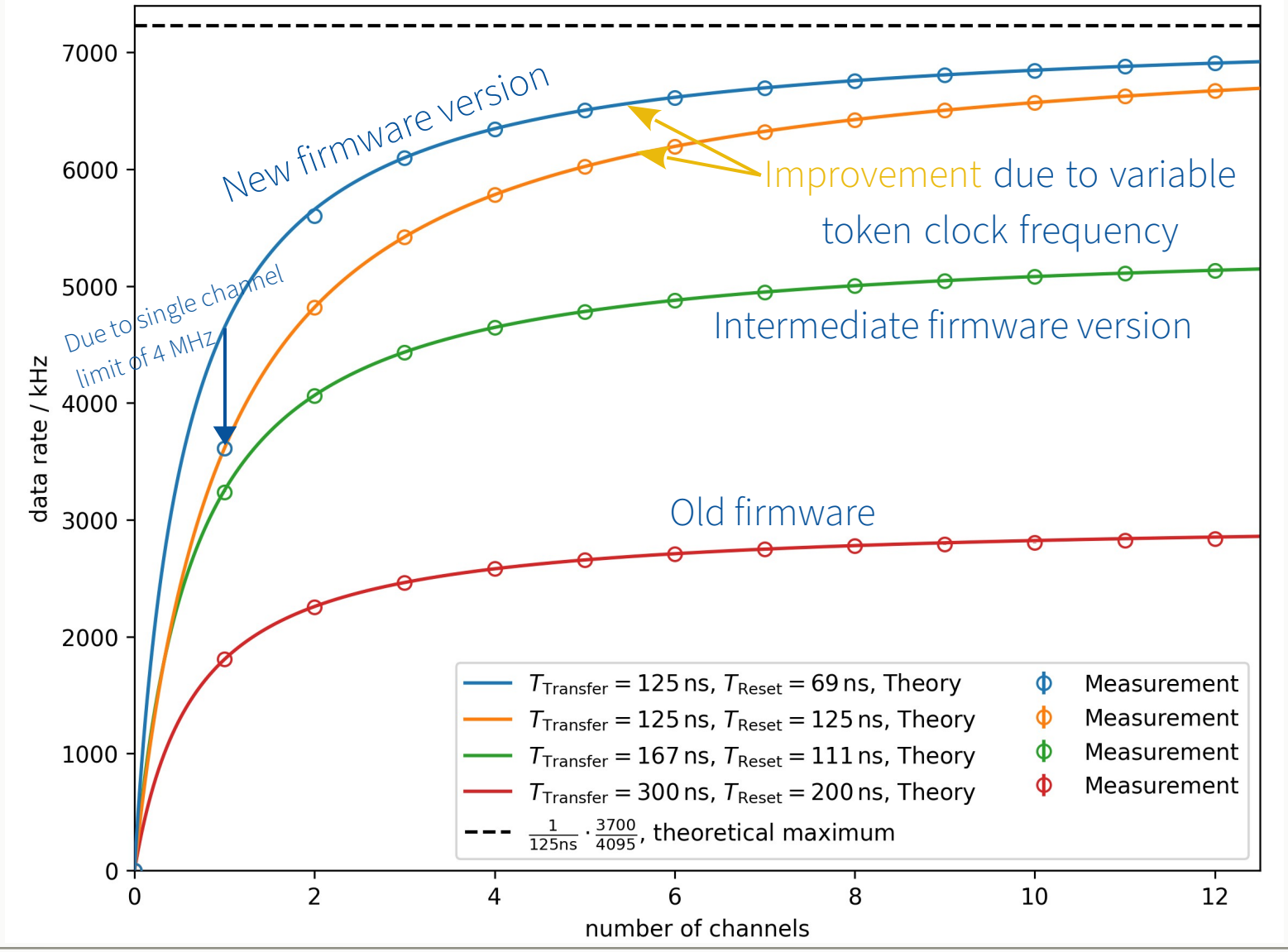
So far unobserved:

gaps between transfers → data rate reduced by (active channels)/(active channels+1)



Reduce impact by sending token earlier, if no data is sent → variable token clock frequency

COMPARISON OF DATA RATES



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SUMMARY

- New data deserialiser for VMM on SRS Hybrid
  - Making 200 MHz DDR data transfers possible
- Decreased transfer time per hit from 300 ns to 125 ns
- Addressed current limitations of VMM:
  - 180 MHz DDR as 200 MHz not working currently
  - Reduction of impact of additional tokens during readout
  - Workaround for need of longer tokens

    → All these adaptions can be removed easily in case VMM is updated

- Bonus:
  - Transfer clock selectable: 180 MHz, 90 MHz, 45 MHz, 22.5 MHz
  - Data deserialiser capable of calibrating itself to align data correctly

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Thanks for your attention!

Questions?