First considerations for a readout system for the ILD TPC with the Timepix3

DPG Hamburg
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Federal Ministry of Education and Research

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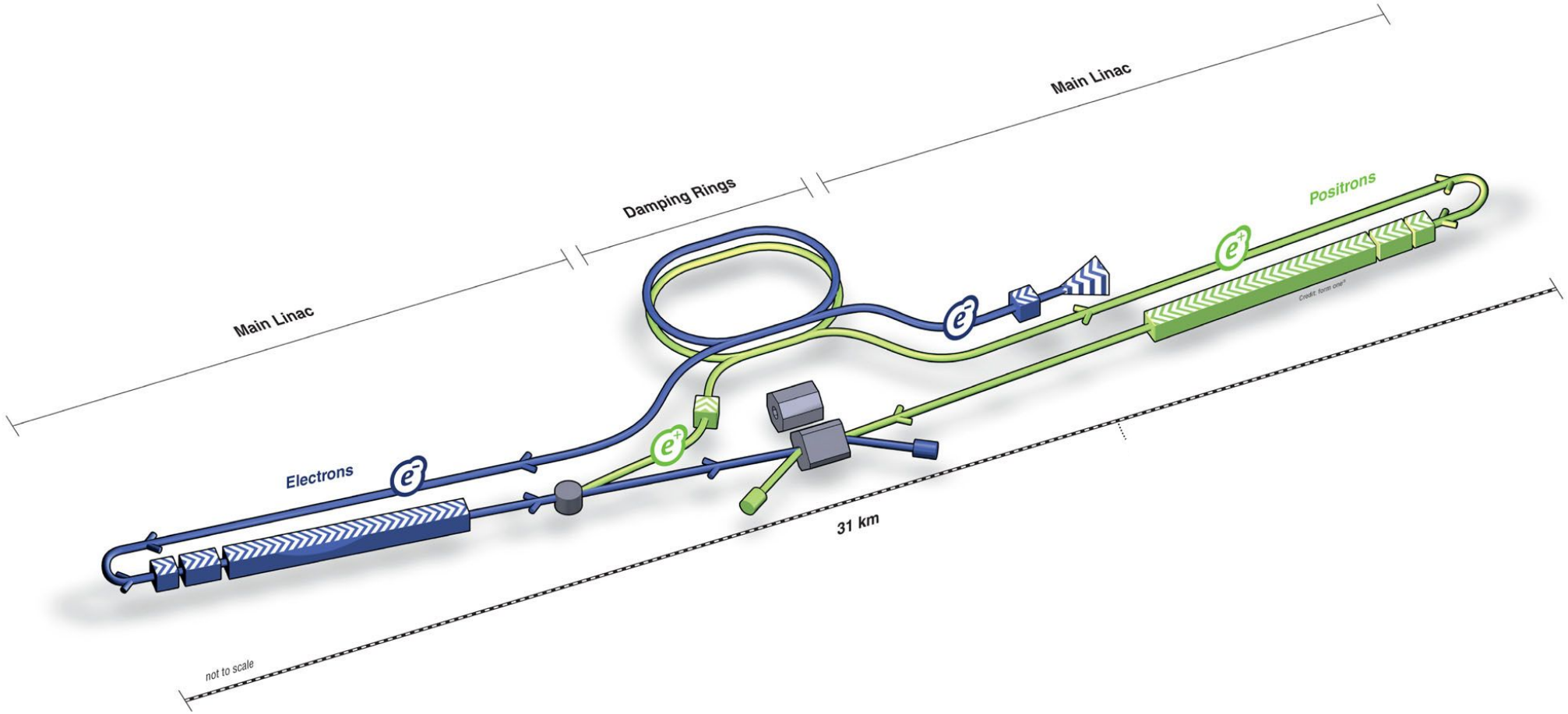
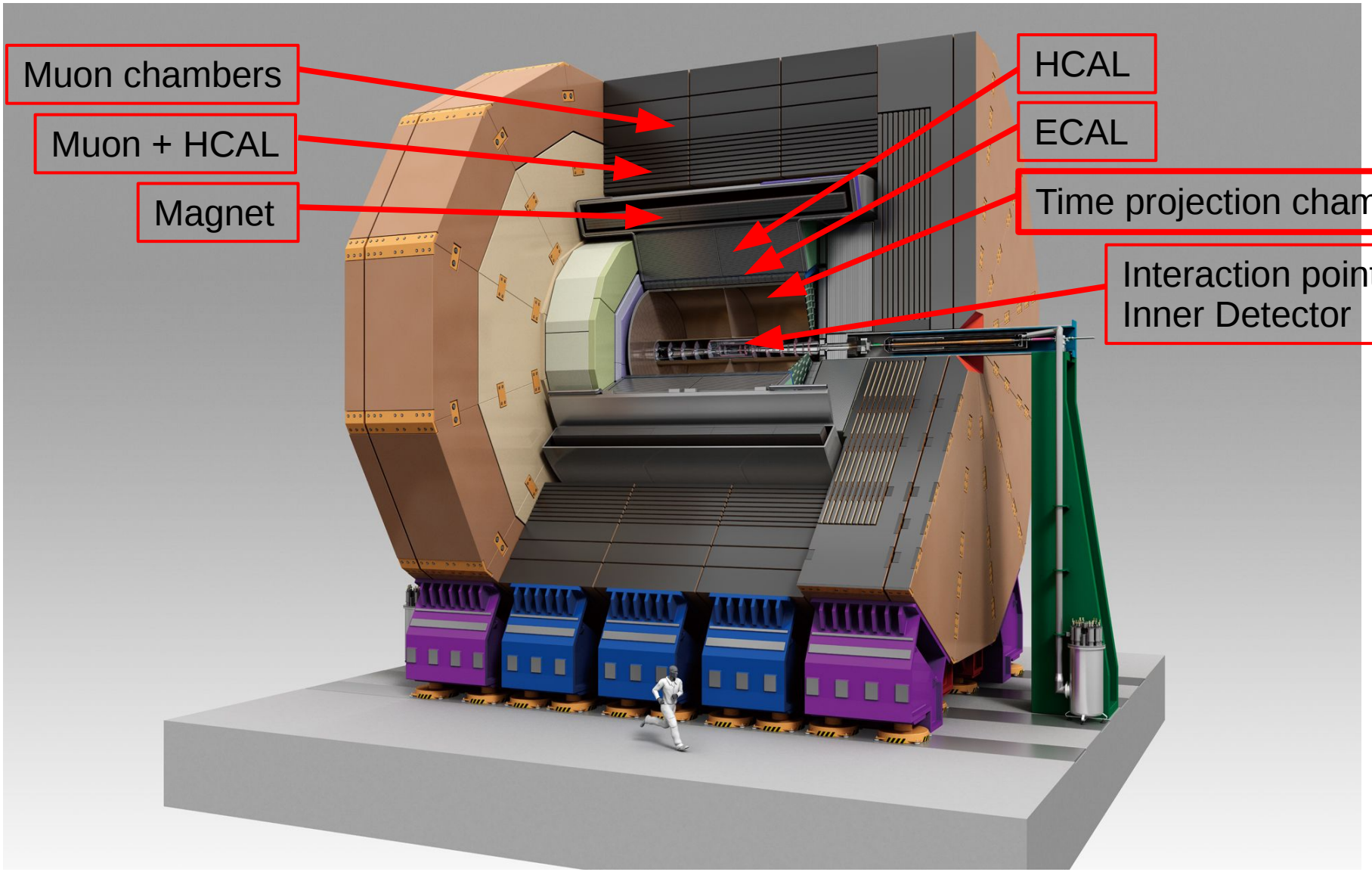
universitätbonn

International Linear Collider

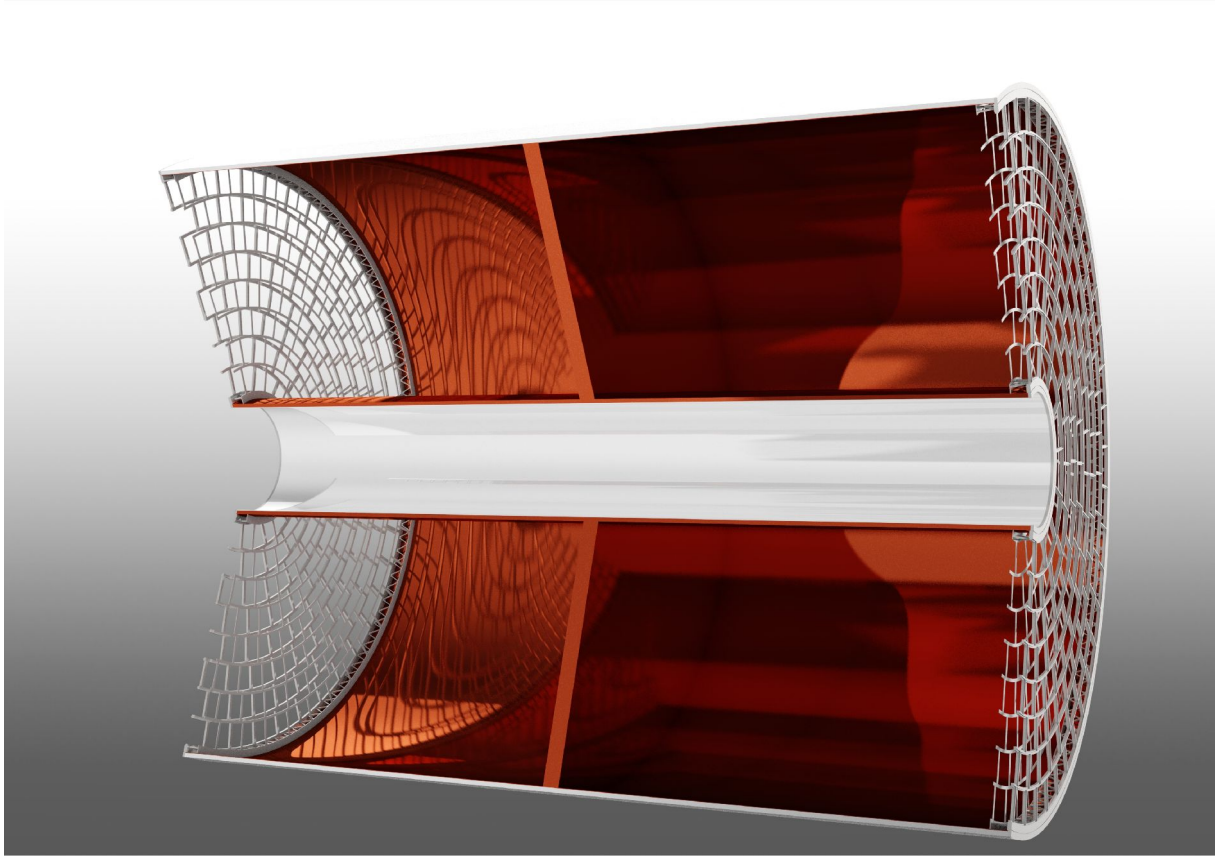
- 500 GeV to 1 TeV future electron positron collider



International Large Detector

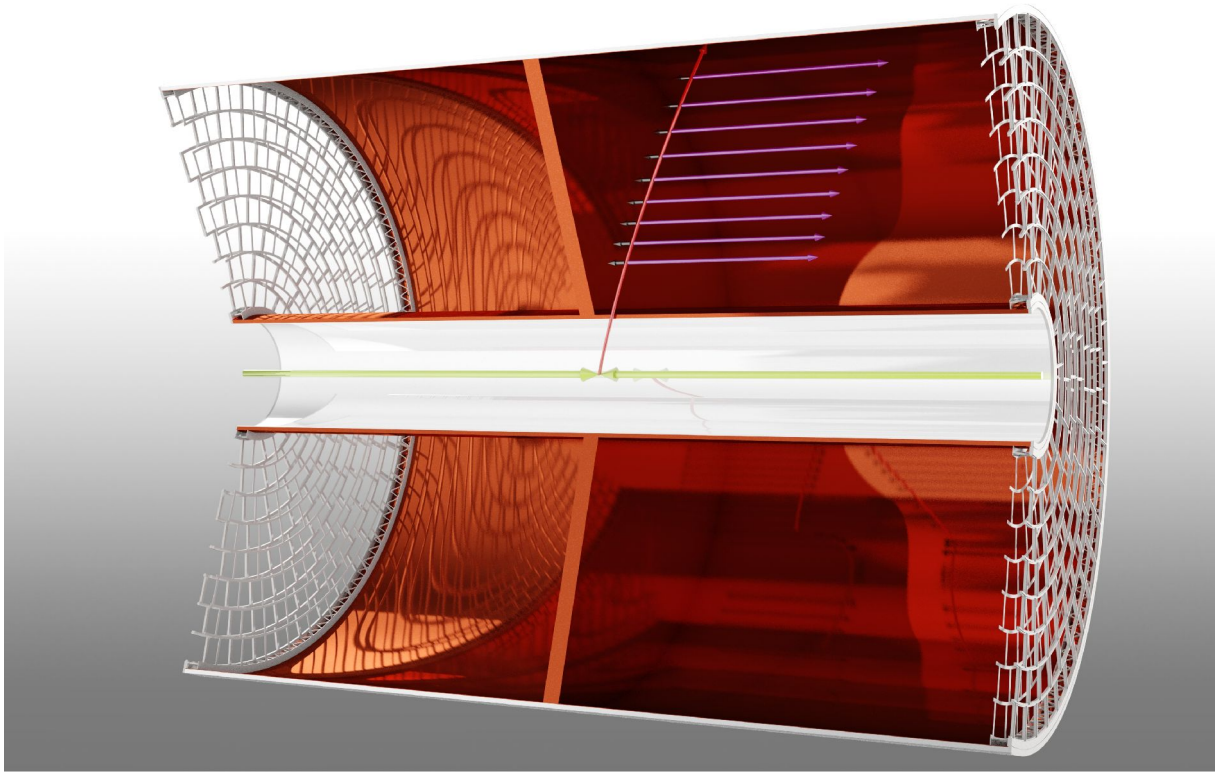


Time Projection Chamber



- Main tracker
- 4.3 m long
- 3.6 m diameter
- 10 m² endplates per side

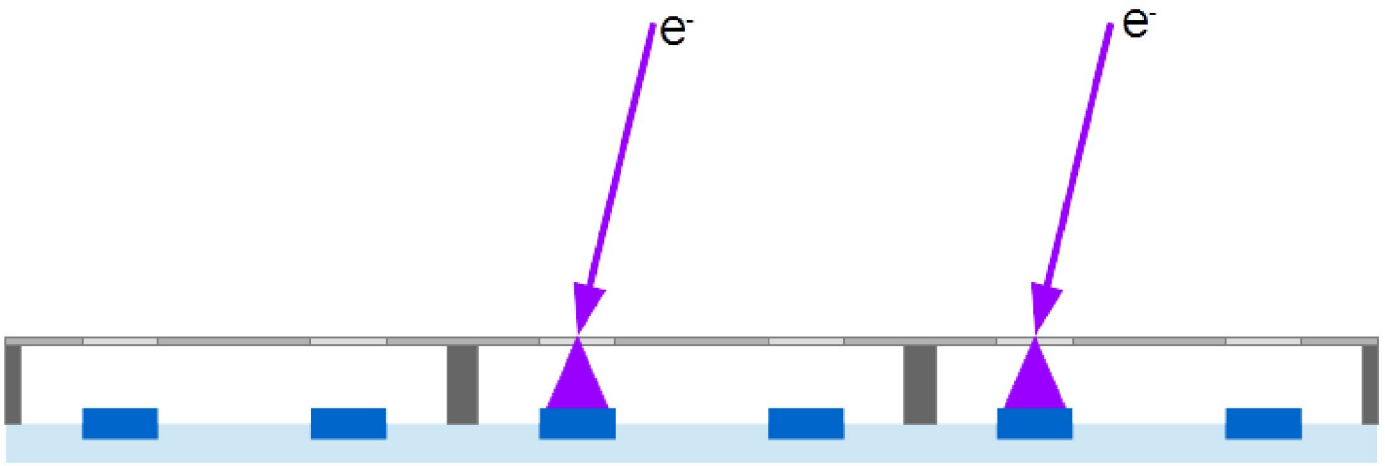
How does this work



- Electrons and Positrons collide
- New particle is produced
- Particle ionises some of the gas atoms
- Electron drifts towards the detector modules due to electric field

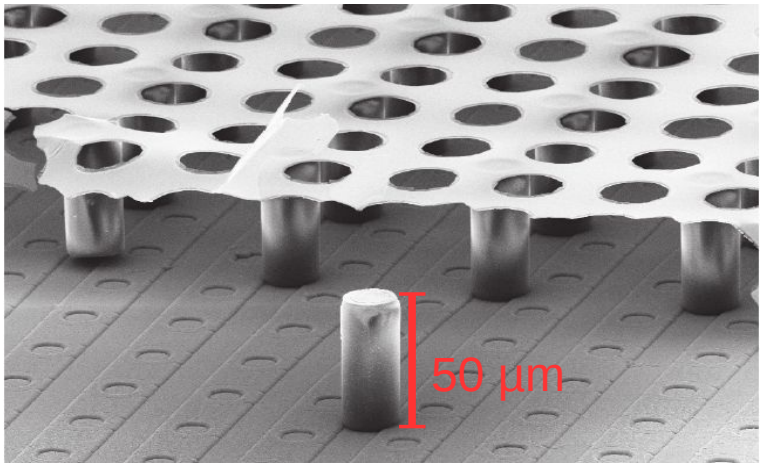
Amplification with the InGrid

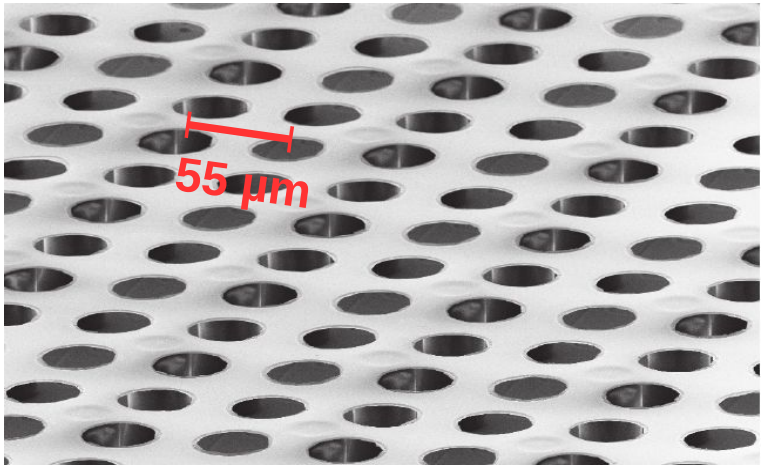
- Below the grid the field is stronger causing an avalanche effect
- Charge is measured in our case with a pixel chip



InGrid

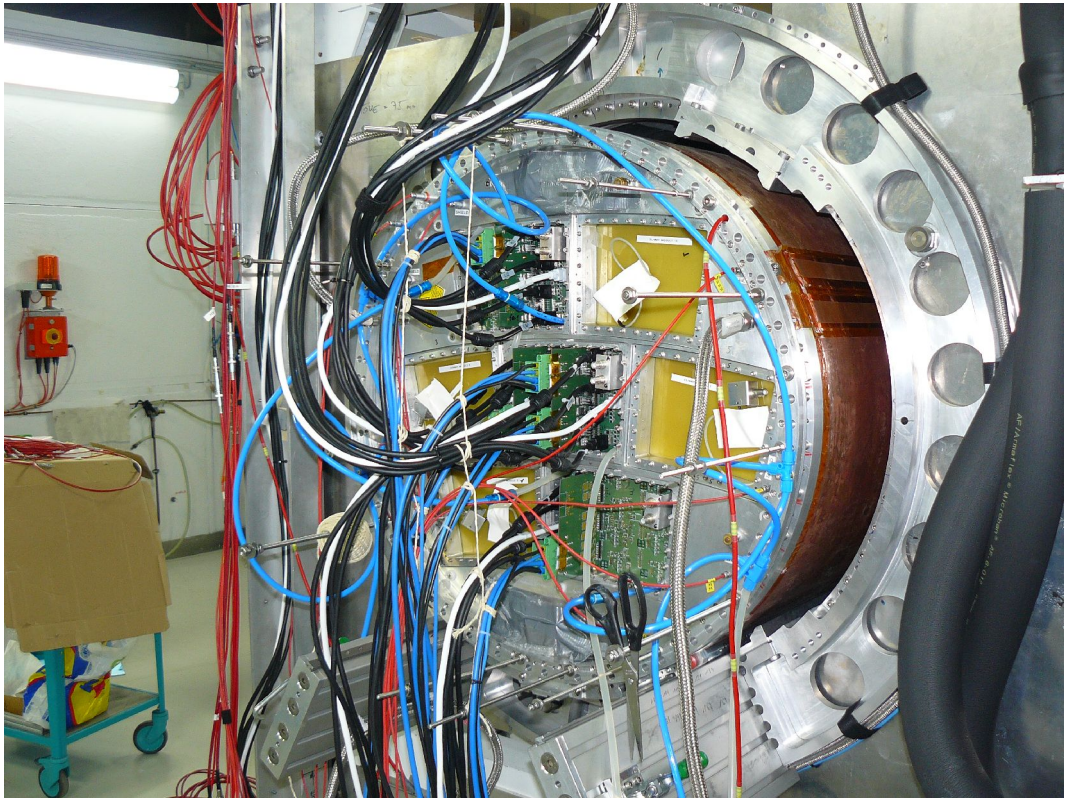
- Micromegas structure
- Aluminium grid of 1µm thickness
- One hole above each pixel
- 55 µm spacing between the holes



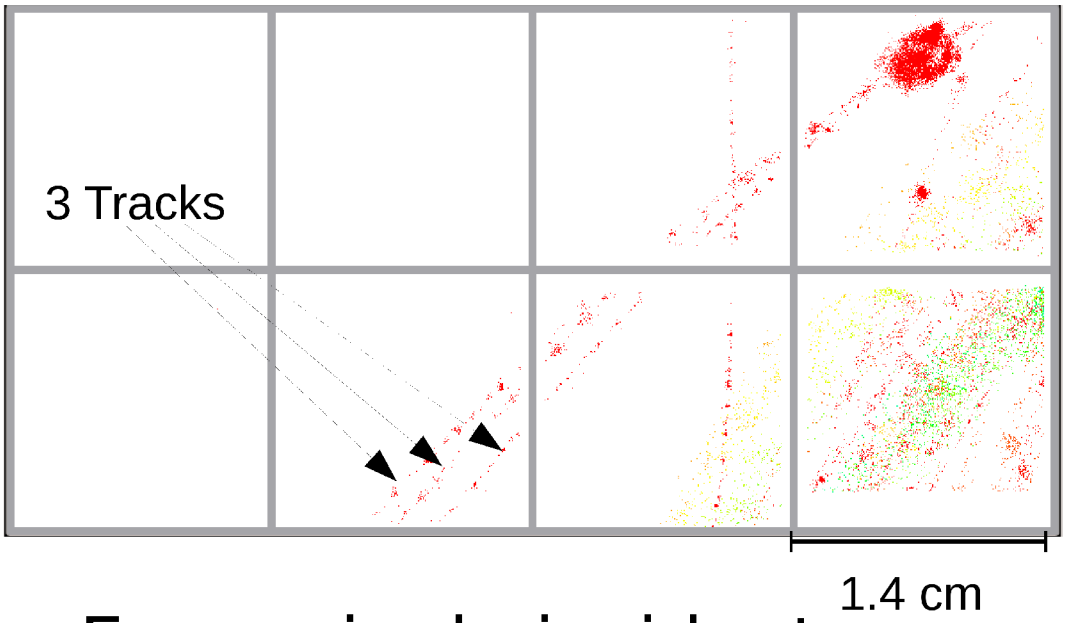


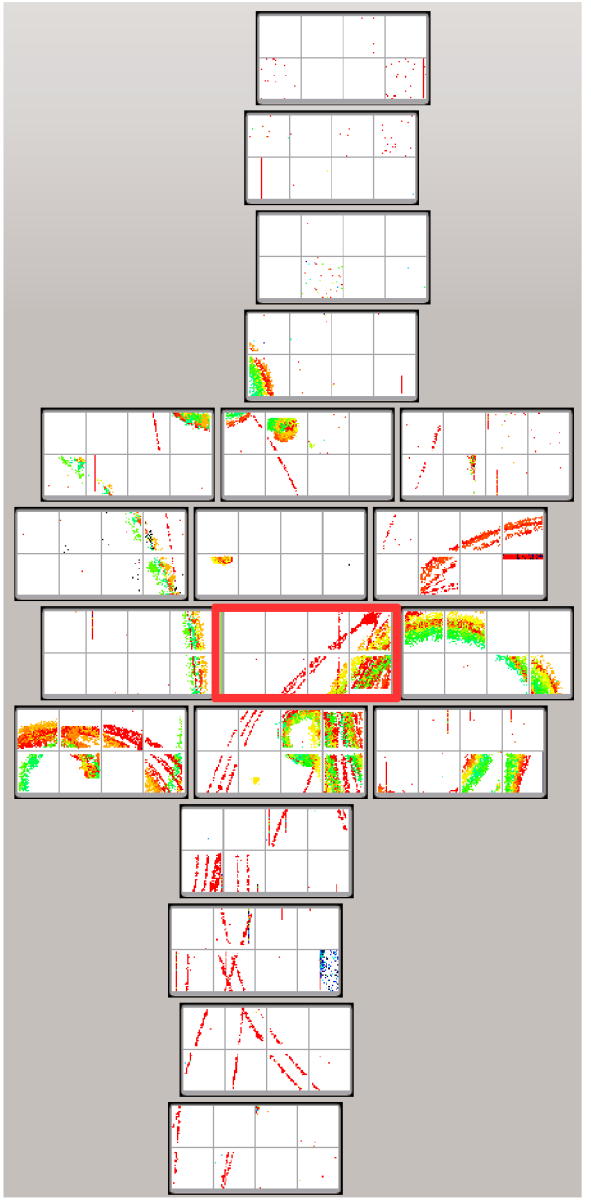
The Timepix setup

- Readout of 160 Timepix ASICs in parallel
- Built by M. Lupberger
- Test in the large prototype at DESY
- Showing good results in testbeam (→ T 73.1)



Measurements with the Timepix

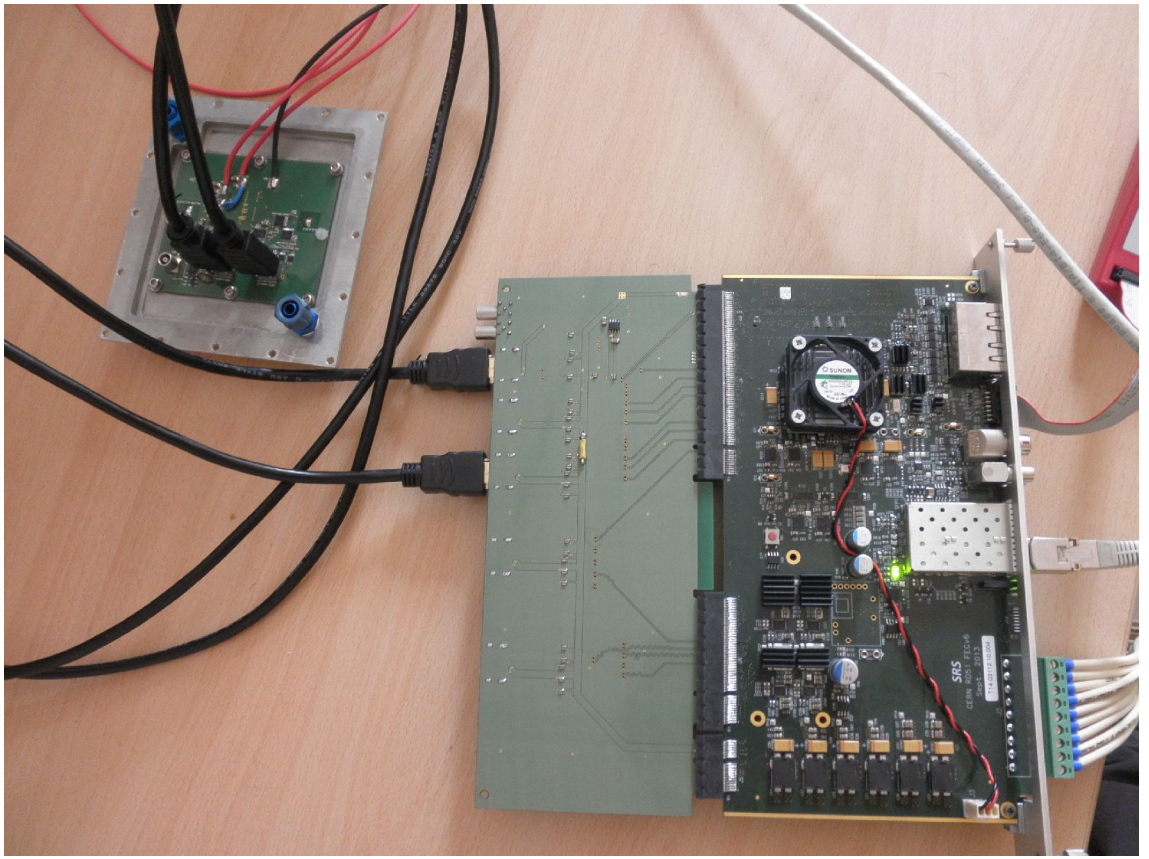




- Every single incident electron visible
- Good separation of close by tracks

High Scalebility

- Using the Scalable Readout System (SRS)
- Readout of 32 ASICs with one FPGA

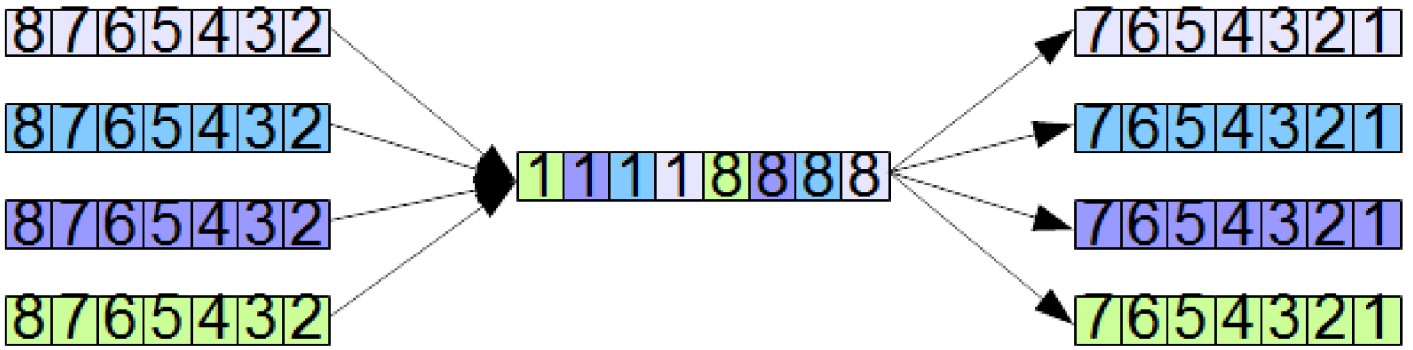


Timepix vs. Timepix3

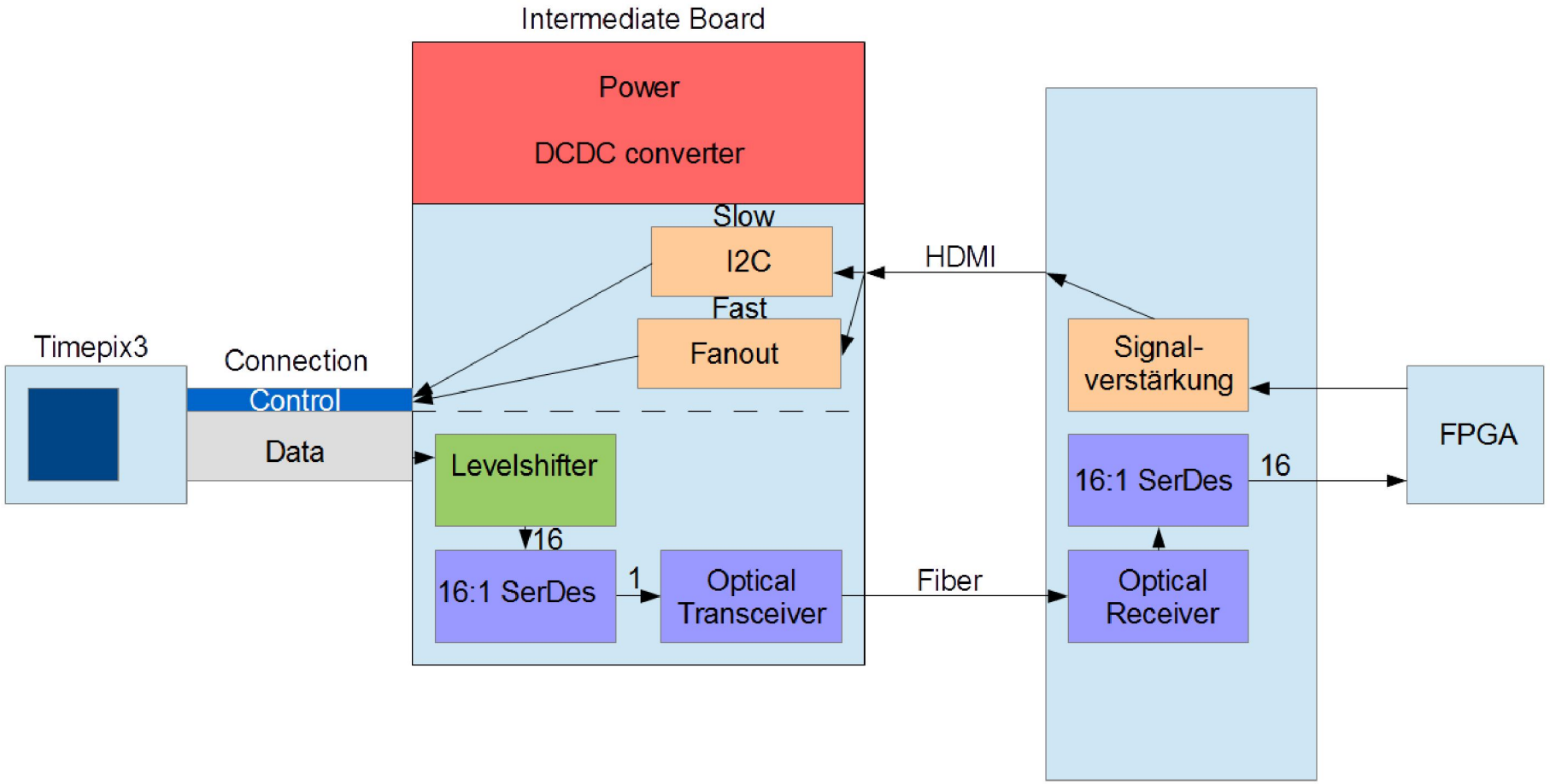
ToT (charge) or ToA (time)	ToT and ToA at the same time
Frame based output	Data driven or frame based output
No zero suppression	Zero suppression
Noise threshhold 750 e^-	Noise threshhold 500 e^-
Time resolution 10 ns	Time resolution 1.5 ns
ENC 90 e^-	ENC 60 e^-

How to read out many Timpix3 ASICs

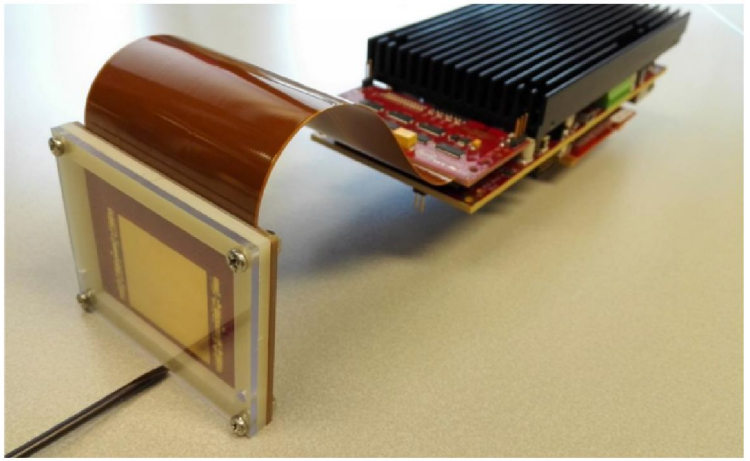
- Concentrator
- Serializing the output of several ASICs
- Connection via fiber-optics
- Using highspeed inputs at the FPGA or deserialize



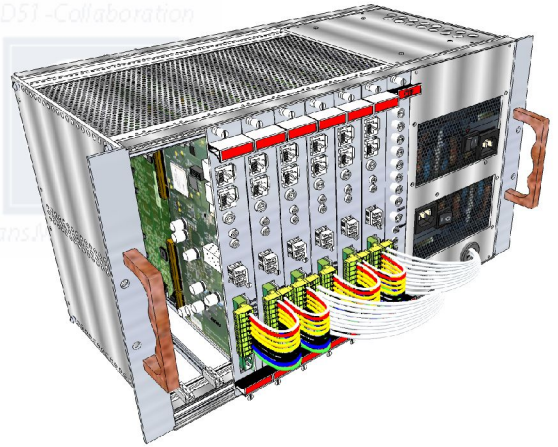
Set-up


Intermediate Board
Power
DCDC converter
Slow
I2C
Fast
Fanout
HDMI
Timepix3
Connection
Control
Data
Levelshifter
16
16:1 SerDes
1
Optical Transceiver
Fiber
Signal-verstärkung
16:1 SerDes
16
FPGA
Optical Receiver

SPIDR vs. SRS



- Small
- High speed
- Specified for 4 Timepix3



- Needs Eurocrate
- Up to 8 FECs per crate
- Highly scalable

Summary & Outlook

- Readout of 160 Timepix ASICs shows good results
- Timepix3 has many advantages
- Concentration is required
- Readout with SPIDR or SRS

- Set-up for the Timepix3 with the SPIDR for testing
- PCB development for serialisation