Production and Application of an Integrated Pixel Readout for a Linear Collider

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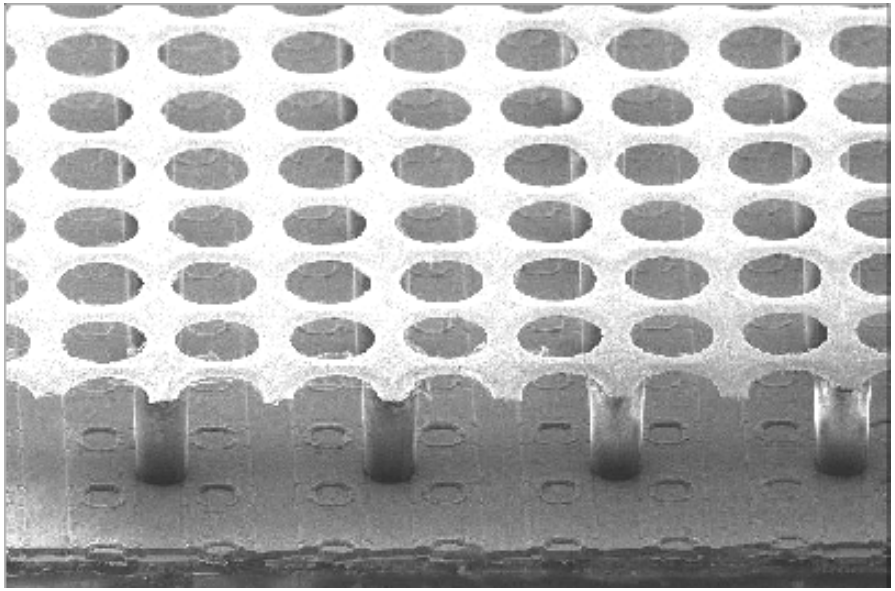
Contents

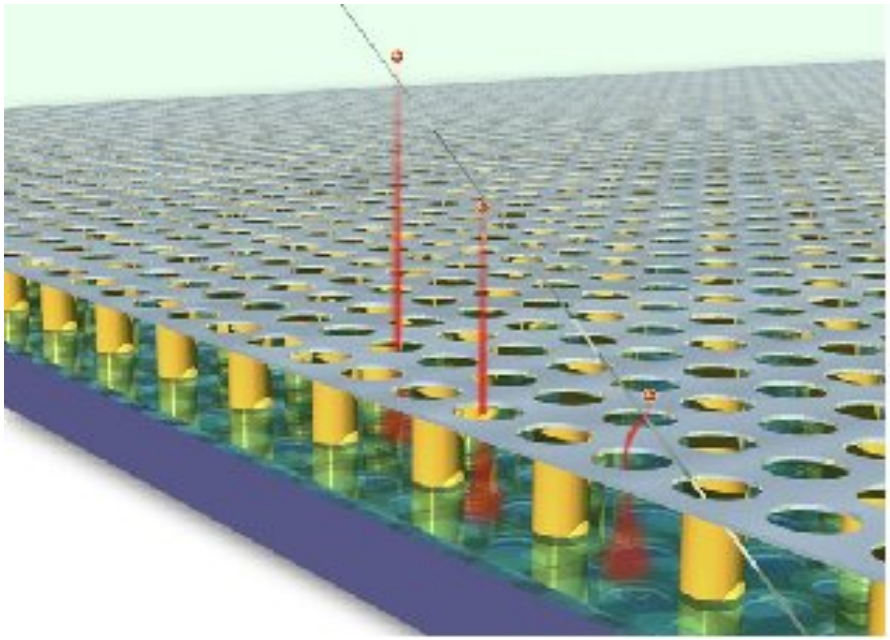
InGrid - Integrated Pixel Readout

GridPix

Micromegas on a pixelchip

- Insulating pillars between grid and pixelchip
- One hole above each pixel
- Amplification directly above the pixelchip





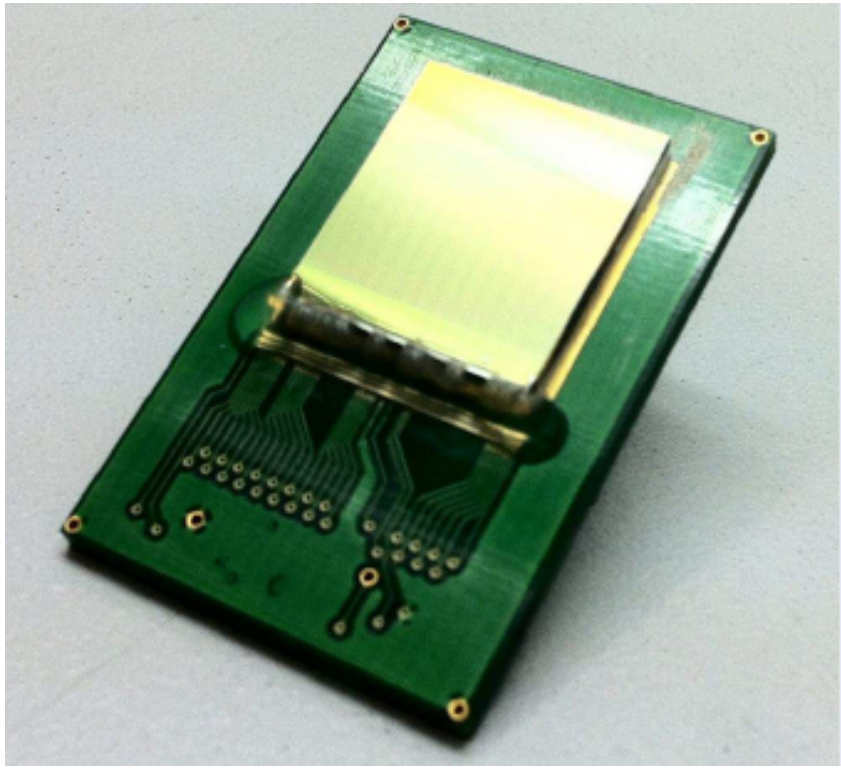
Advantages

- Very high single point resolution
- Perfect alignment
  - Each primary e^- is detected on one pixel
  - Nearly 100 % single e^- efficiency
  - Low occupancy

Timepix Pixel Chip

Characteristics

- Derived from Medipix-2
- 256×256 pixel
  $\Rightarrow$ 55 µm pixel pitch
  $\Rightarrow$ 2 cm^2 active area
- Charge sensitive amplifier and discriminator in each pixel
- ENC $\approx$ 100 electrons
- Threshold $\approx$ 700 electrons
- 30 - 100 MHz clock frequency
- Two modes of measurement (per pixel):
  $\Rightarrow$ Time or charge
- No multiple hit capability



Successor: Timepix-3

In preparation

- Simultaneous charge and time measurement
- Multiple hit capability
- 100 MHz with 640 MHz fast clock

Production on Wafer Scale

Single chip production

Production of single (few) chips pioneered and optimized at University of Twente / MESA+

Demand

HEP-Detectors (e.g. ILD):

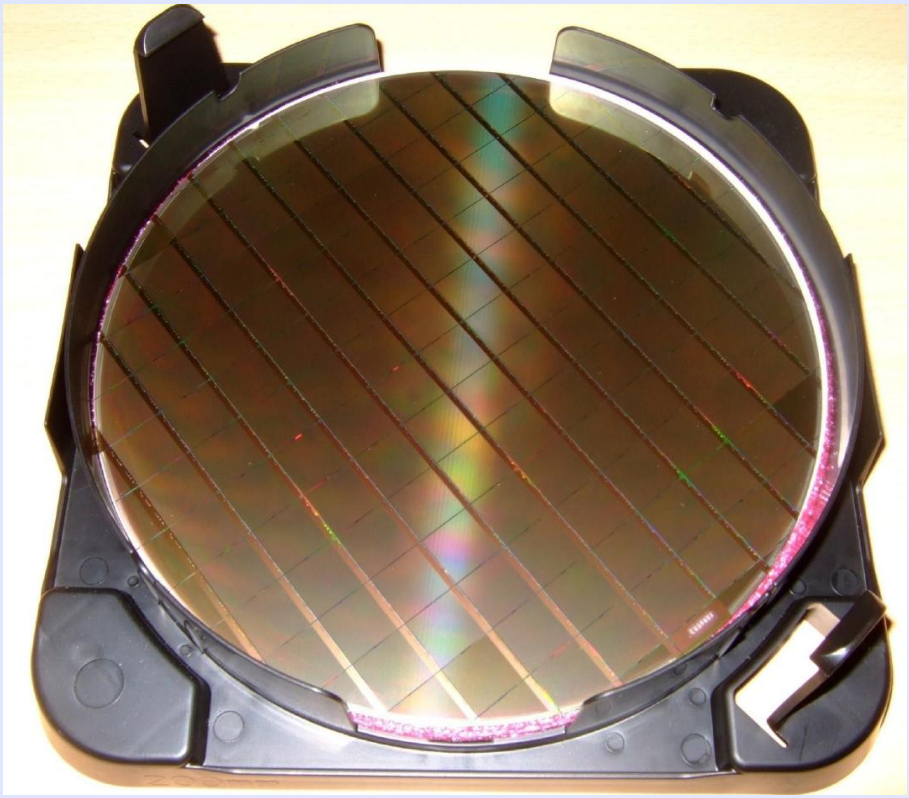
- Readout area of the TPC: $\approx 10\ \mathrm{m}^2$
- Pixelchips ($1.4 \times 1.4\ \mathrm{cm}^2$): $\approx 4 \cdot 10^4$

Research and development:

- Bonn, NIKHEF, Saclay, ...

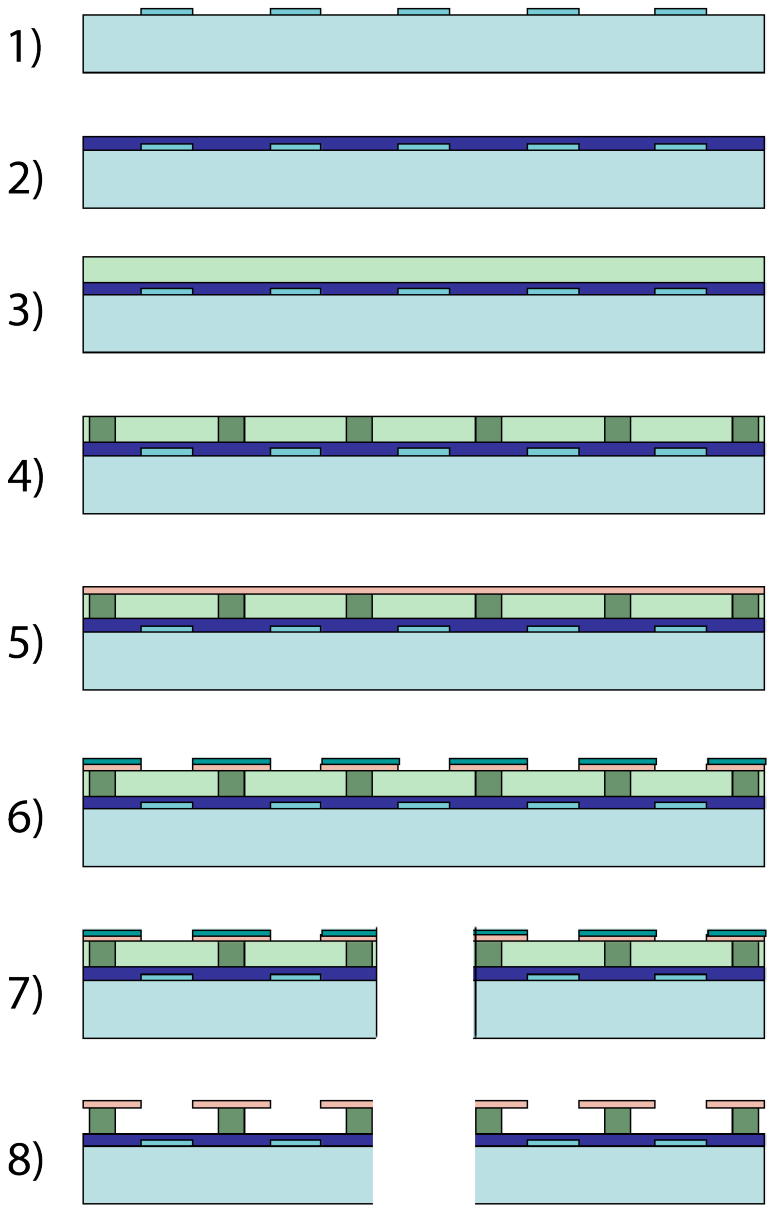
$\Rightarrow$ Production on wafer scale

Timepix wafer

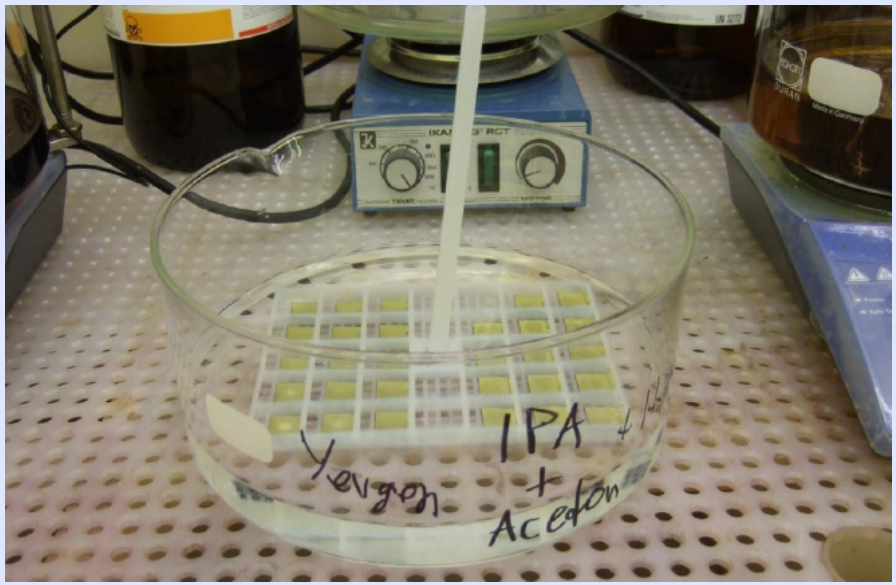


- 8 Inch wafer
- 107 Chips

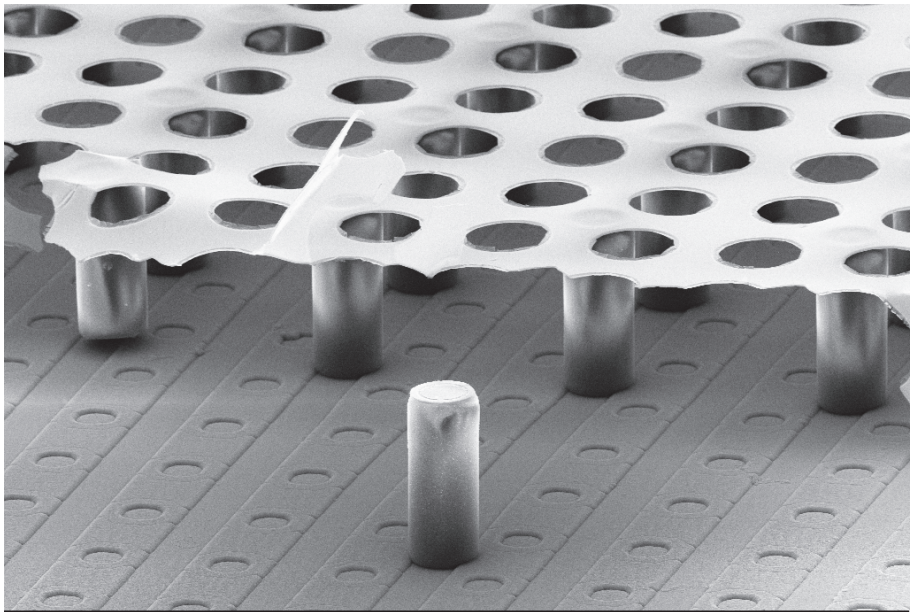
Production on Timepix Wafers

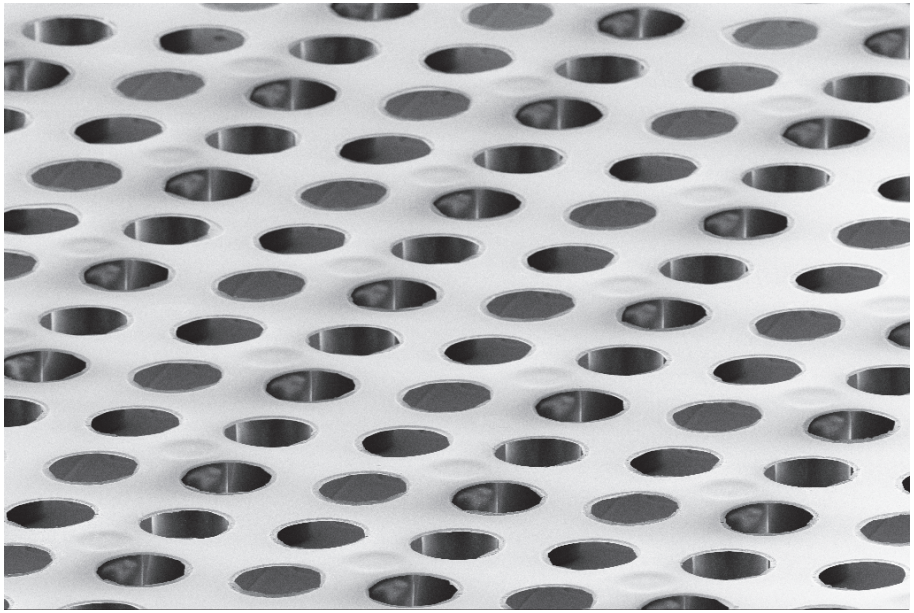


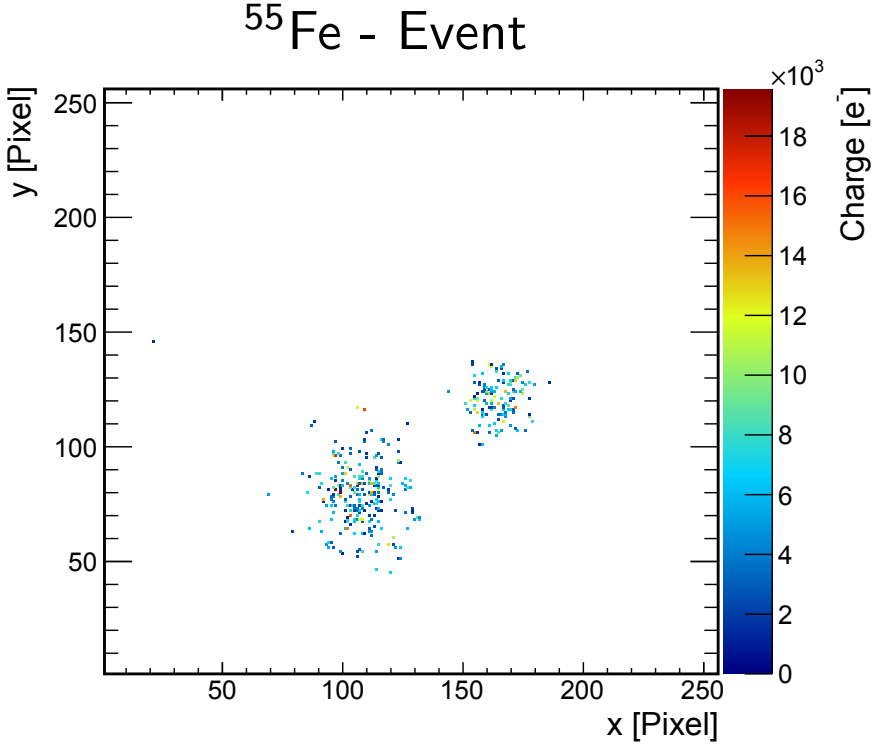
1. Probing and cleaning of the wafer
2. Adding Si_xN_y protection layer
3. Application of the SU-8
4. UV-Exposure of the SU-8
5. Application of the grid
6. Patterning of the grid
7. Dicing of the wafer
8. Development of the SU-8



Production Results



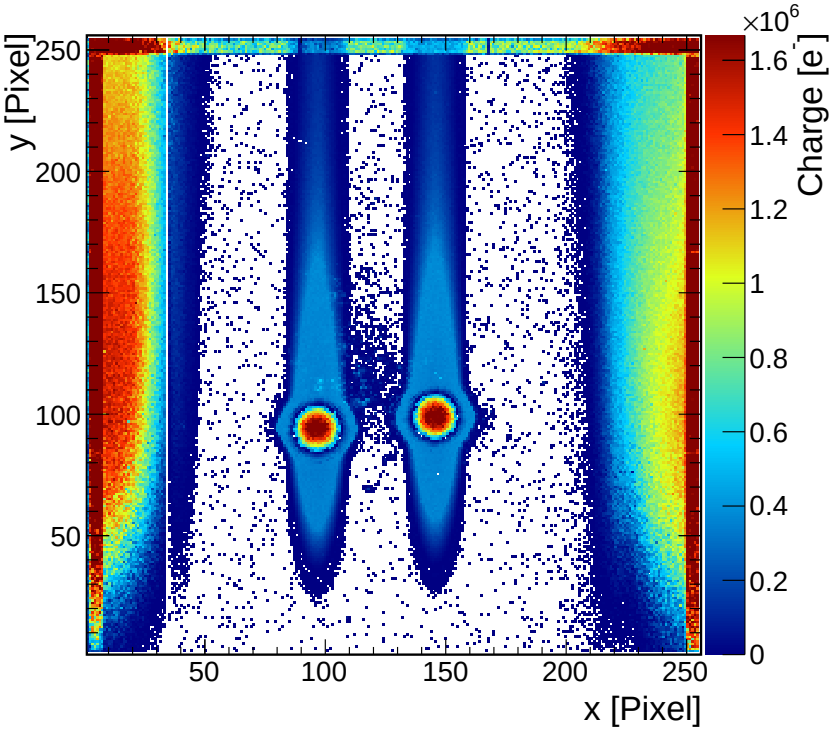


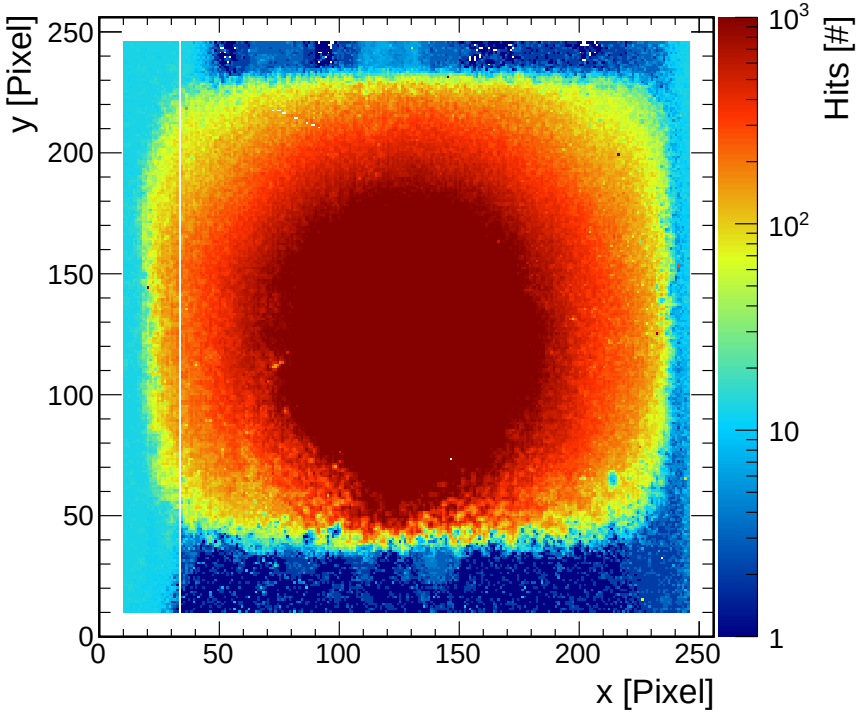


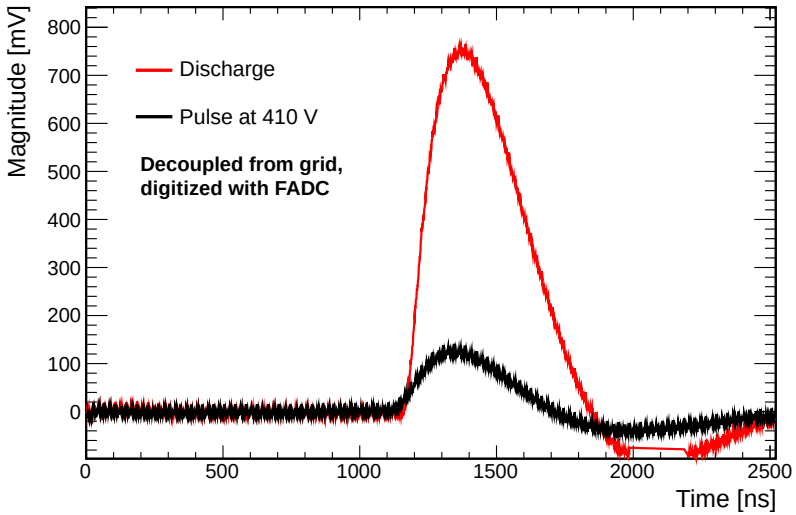
Characteristics

- Occupancy
- Gain
- Energy resolution
- Discharge stability

Occupancy and Discharge Stability





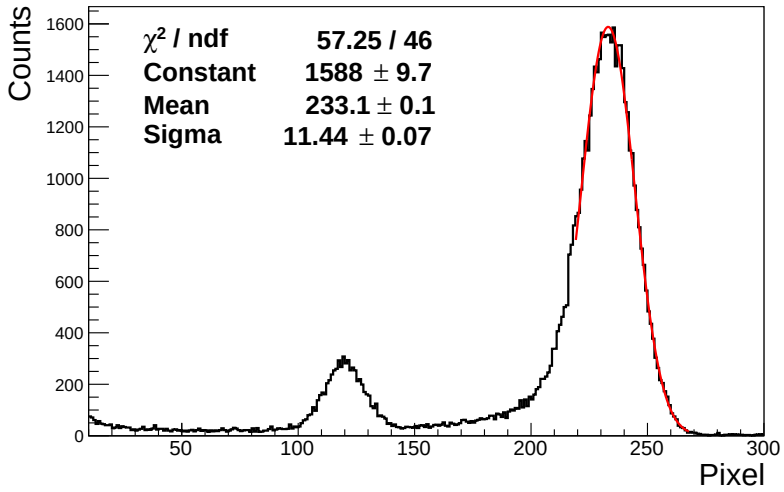


Performance

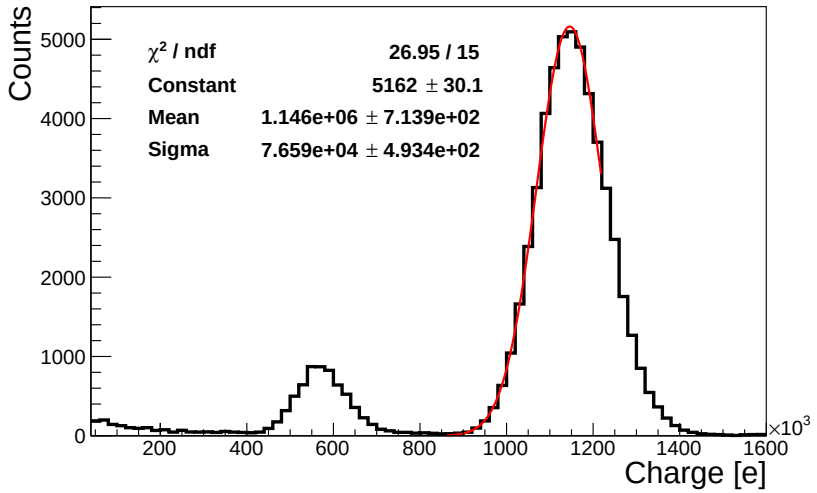
- $\mathcal{O}(10^4)$ X-ray induced discharges
- Grid voltages of up to 450 V in Ar/iButane (95/5)
- But: 7/10 chips destroyed in hadronic test beam at CERN
- Very few closed holes

Gain and Energy Resolution

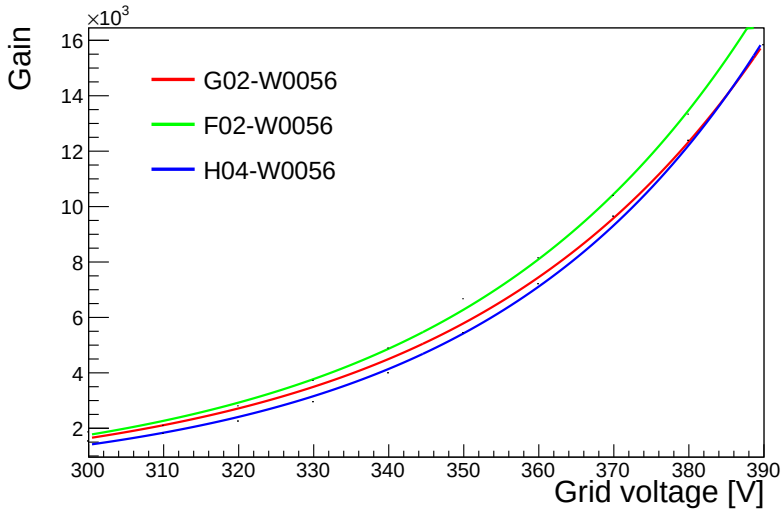
Pixel spectrum



Charge spectrum



Amplification

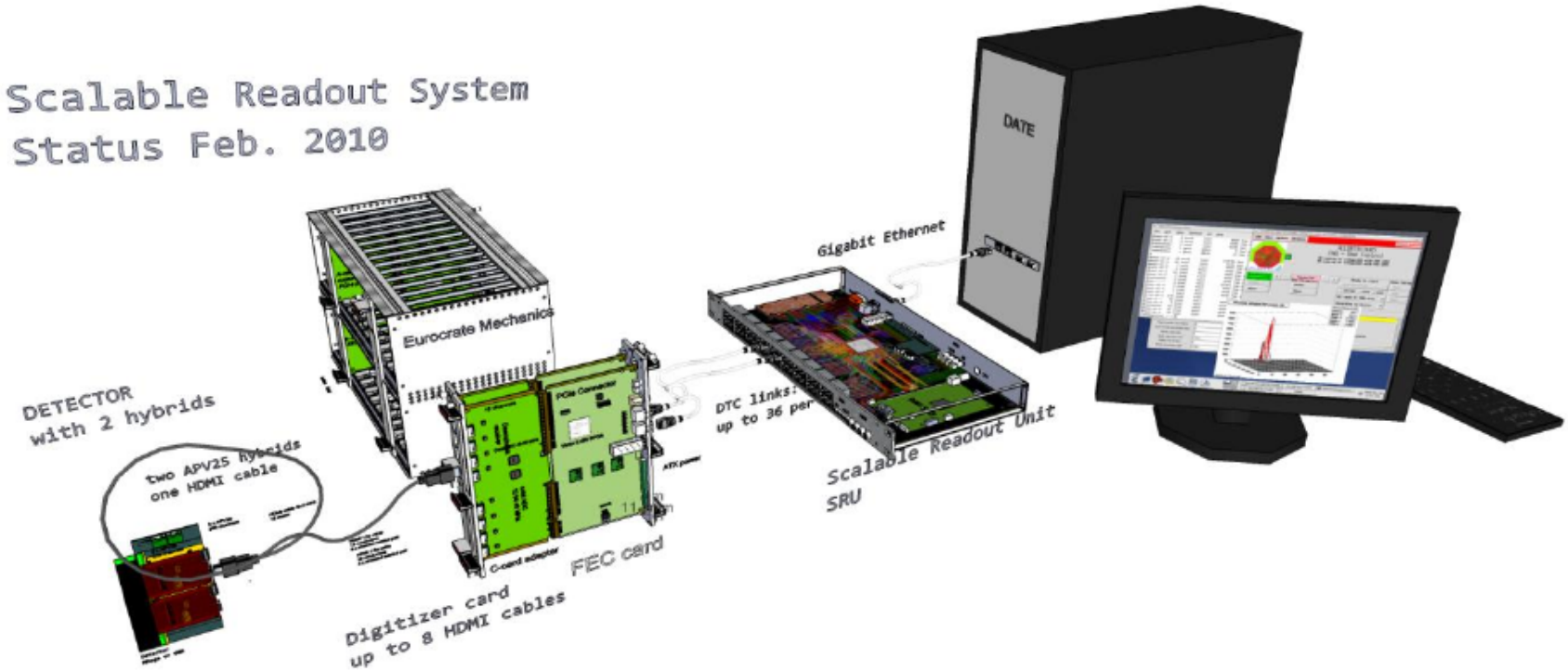


Performance in Ar/iButane (95/5)

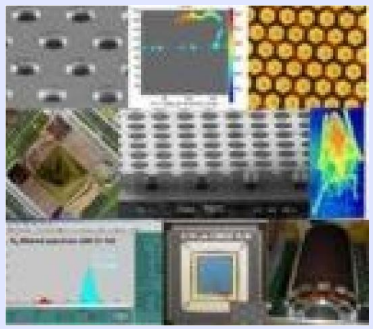
- Energy resolution:
  - Pixel: $\frac{\sigma_N}{N} = 5.0\%$
  - Charge: $\frac{\sigma_N}{N} = 6.7\%$
- Similar Gain for various devices

$\Rightarrow$Performance similar to single chip production

SRS - Scalable Readout System



- Designed by RD51 collaboration with CERN as main developer
- Flexible readout electronics, can handle different frontends (adapt FPGA code, chip carrier)
- High scalability

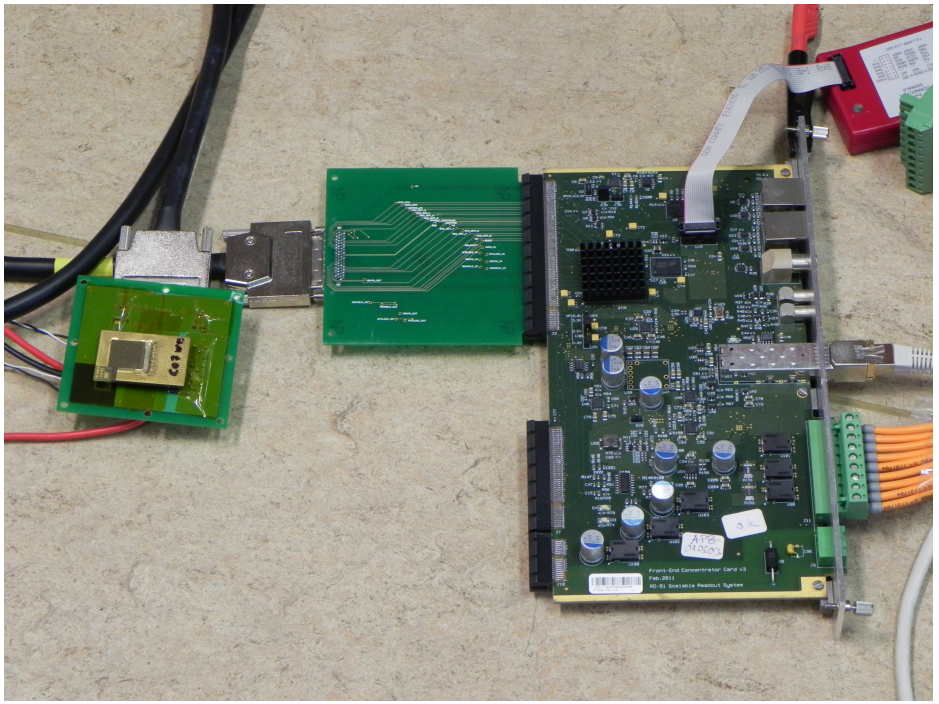


Timepix Readout with SRS

Timepix readout

Development of a SRS based Timepix readout by U. Bonn and U. Mainz

- Adaption of FPGA code on FEC
- Passive routing on adapter board

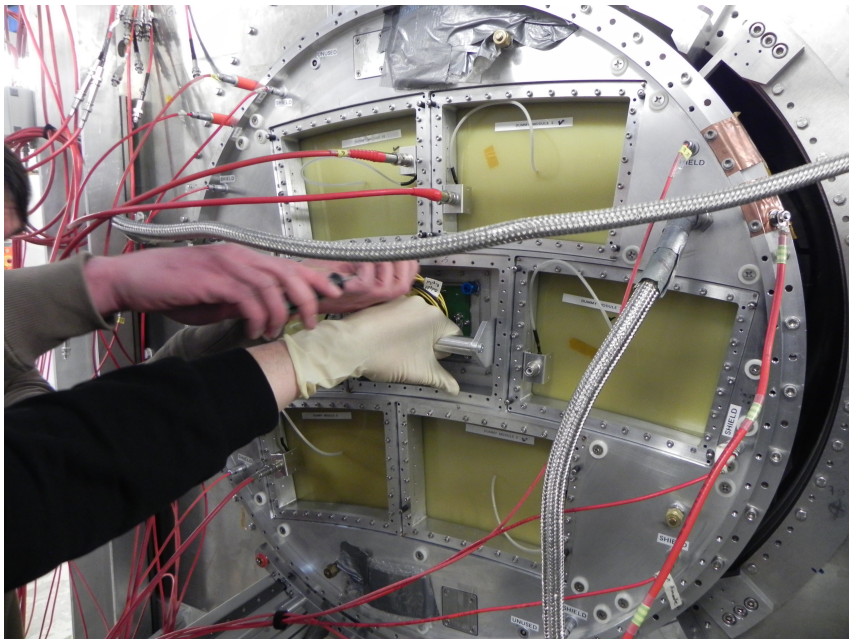


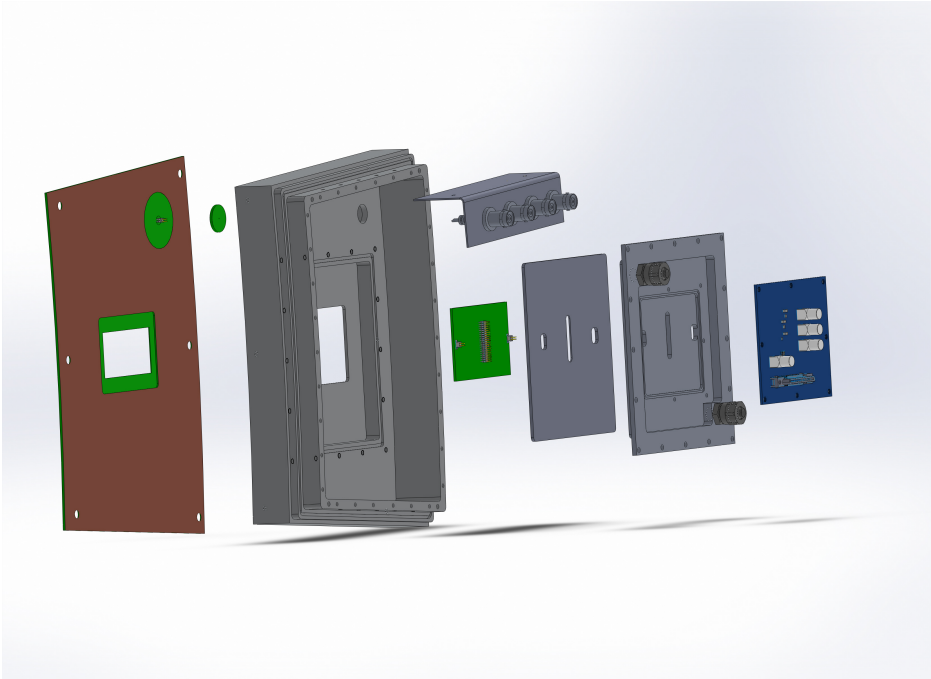
Status

Most function of previous systems (e.g. MUROS) implemented

- Support for 1-8 chips
- Setting of matrix and DACs
- Readout of the matrix
- Threshold equalization
- External test pulses
- Calibration

The Octoboard - A Module for the Large Prototype

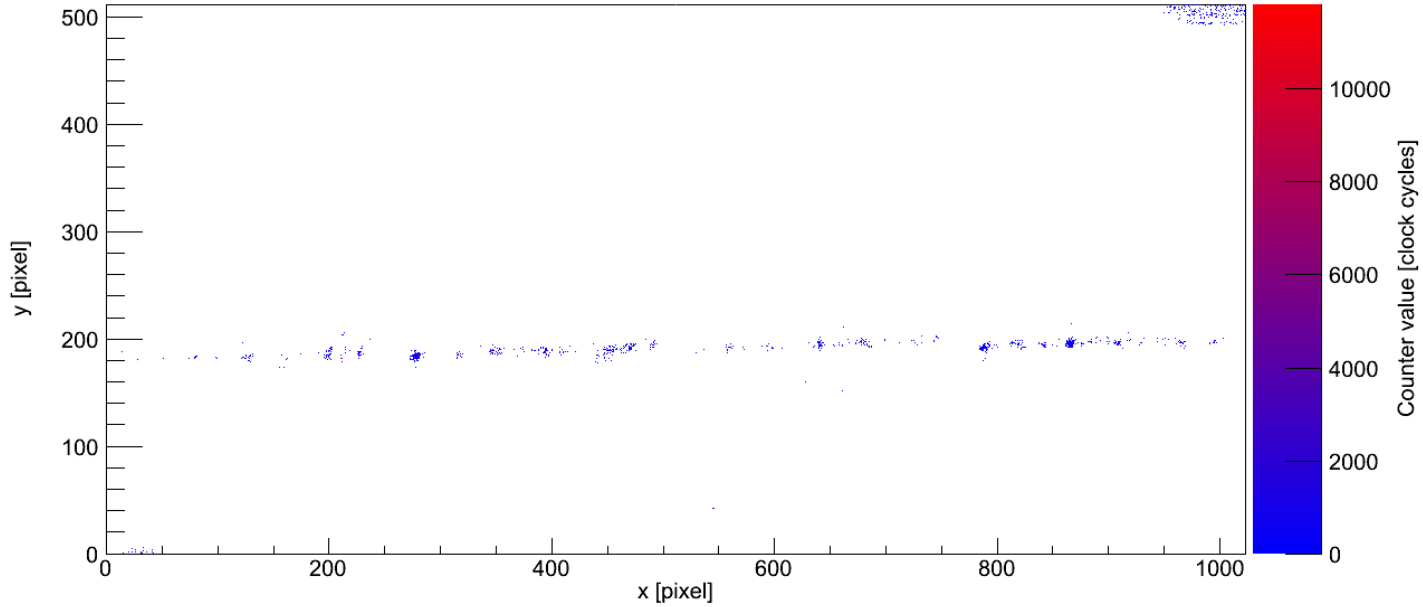


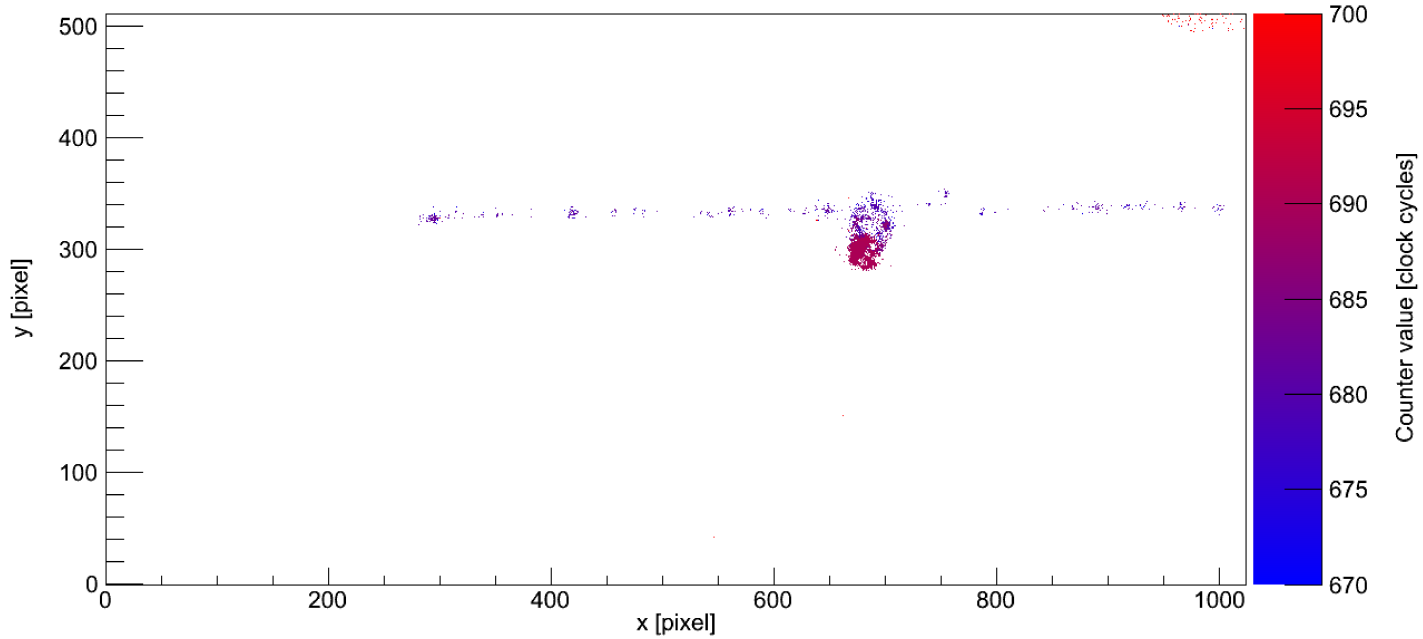


Octoboard: LP module

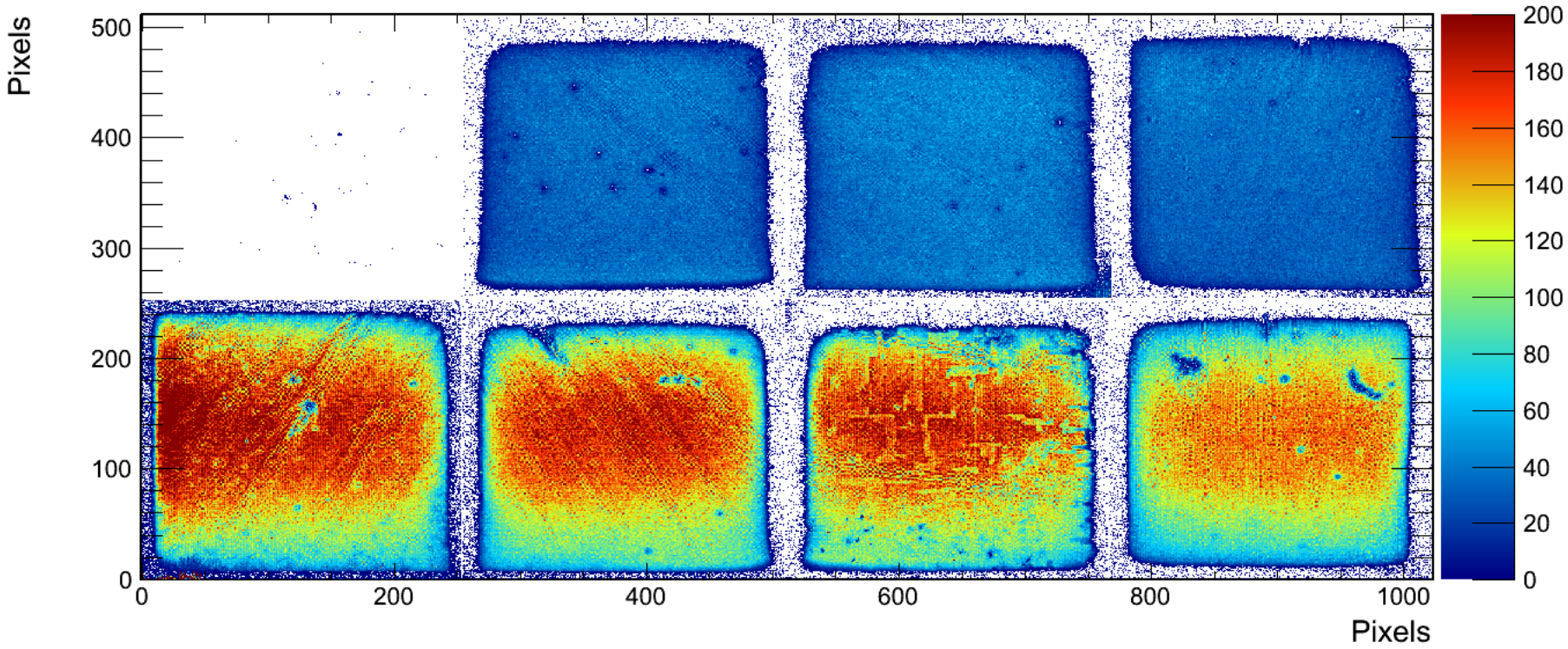
- Module for Large Prototype TPC at DESY
- 8 chips on one board
- Readout with SRS

Example Events





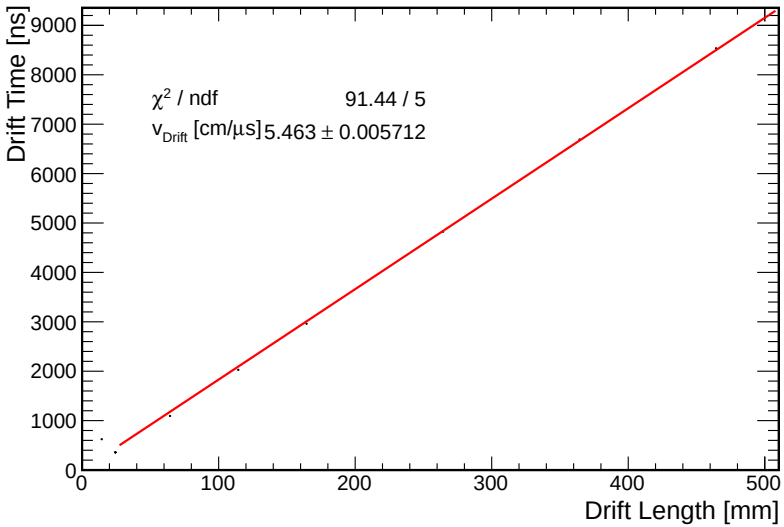
Occupancy



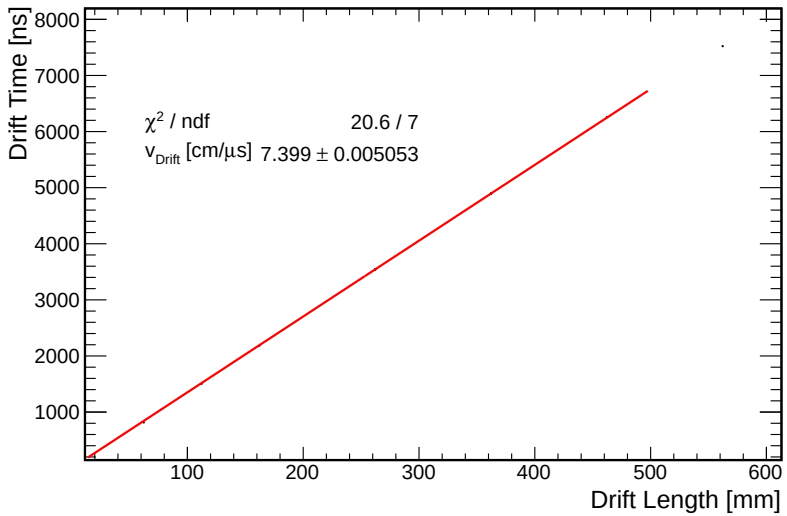
- One chip not equalizable (under investigation)
- Some unresponsive spots in the active area of the chip

Drift Velocity

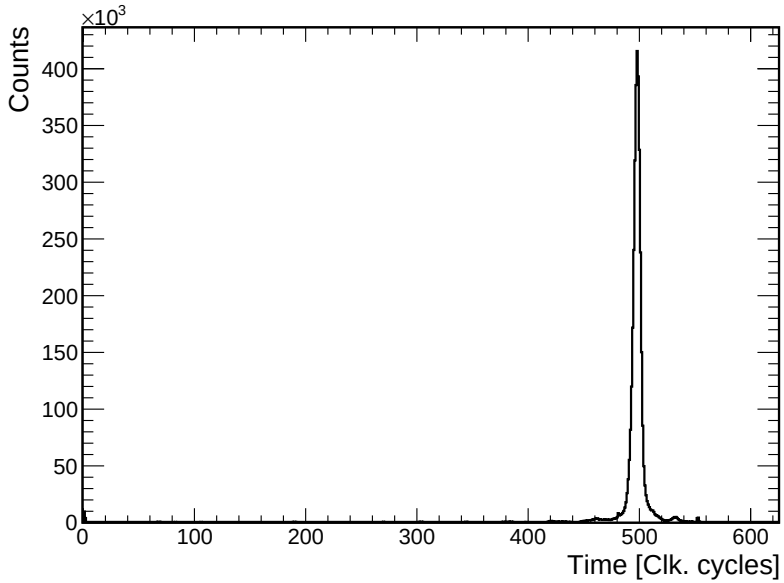
E = 130 V/cm



E = 230 V/cm



Drift spectrum



Velocity in T2K gas

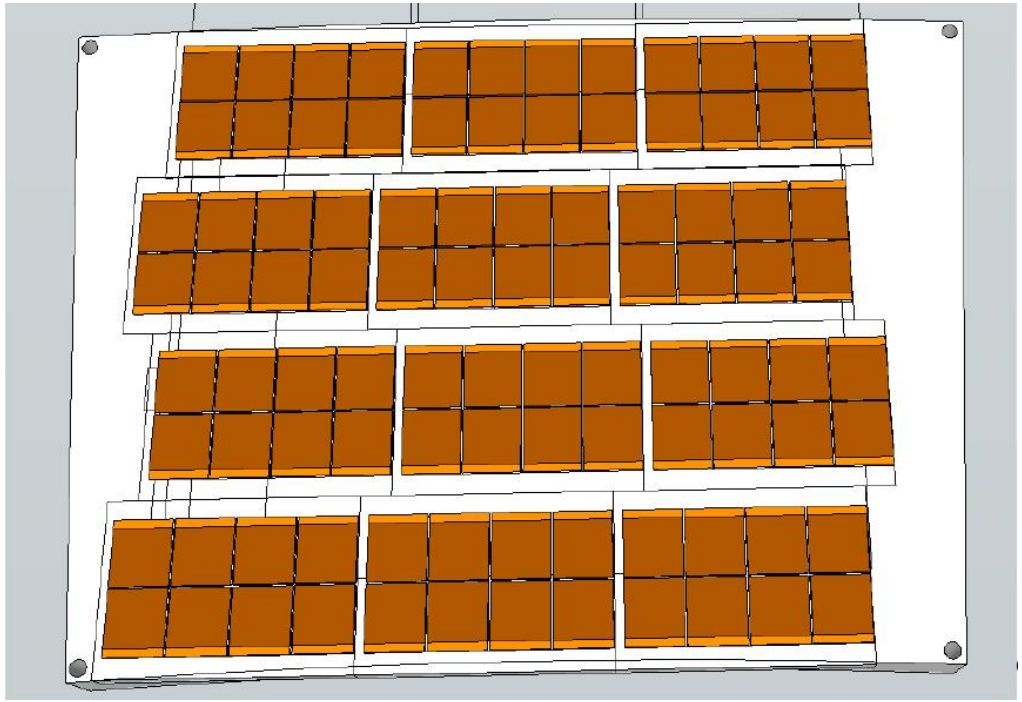
Good agreement with Magboltz simulation

- $v_D = 5.526 \pm 0.003$ cm/µs at $E_D = 130$ V/cm
- $v_D = 7.602 \pm 0.003$ cm/µs at $E_D = 230$ V/cm

Next Step: Large Area Module with $\mathcal{O}(100)$ Chips

First ideas:

- LP Module with 4×3 octoboards $= 96$ chips
- Staggered placement
- Active area $\approx 50\%$



Preparations

- 4 octoboards per FEC
- HDMI for VHDCI cabling
- FPGA code extensions
- Cooling

Summary

- Wafer scale production successful
  - Performance similar to single chip production (Amplification, energy resolution ...)
  - Good discharge stability
- New readout based on SRS
  - Fully operational for 1 to 8 chips
  - Preparations for more chips ongoing
- Octoboard
  - Successful test beam
  - Detailed analysis ongoing
- Next step: Construction of a module with about 100 chips