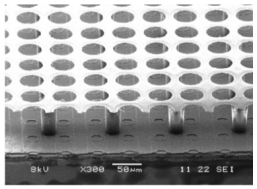
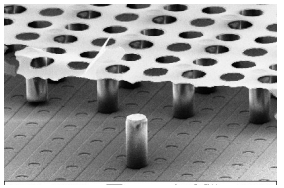




Pixelized TPC readout - status and prospects

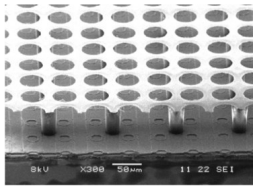
Y. Bilevych, C. Brezina, K. Desch, *J. Kaminski*,
T. Krautscheid, C. Krieger, M. Lupberger
University of Bonn

F. Müller
DESY, Hamburg

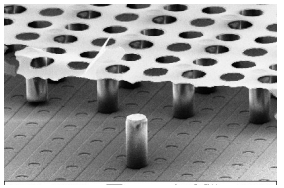
in collaboration with NIKHEF (J.Timmermans) and
CEA Saclay (D. Attie, A. Chauss, P. Colas, M. Titov)

TPCs at high rate experiments
Bonn
1.3.2013

universitätbonn



Content

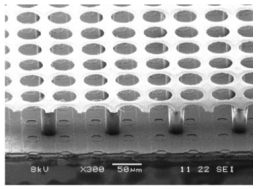


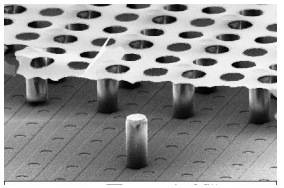
I. Motivation for highly pixelized readout

II. The Ingredients: Chip, Protection Layer, Grid, Detector, ...
- Timepix, Readout Electronics, Software
- Production of grids
- Protection layer
- Some results

III. Necessity for operation in large scale experiments
- New chip
- Industrial production of Grids
- Readout electronics

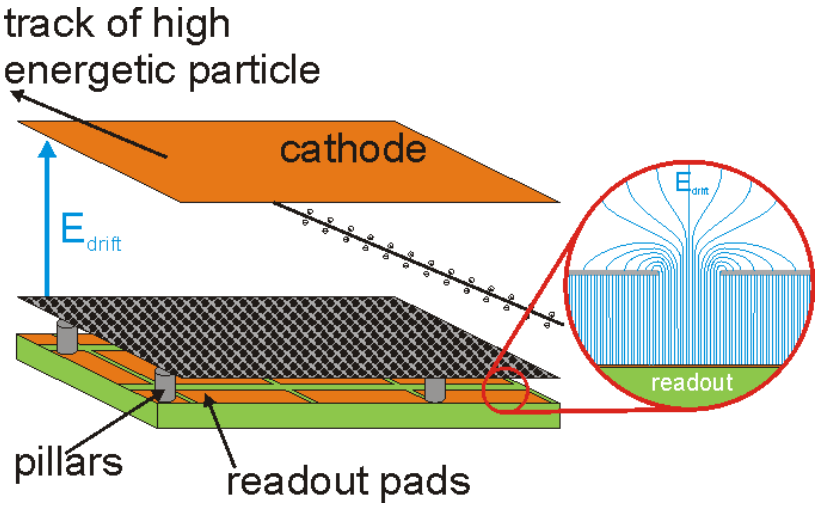
IV. Summary and Outlook

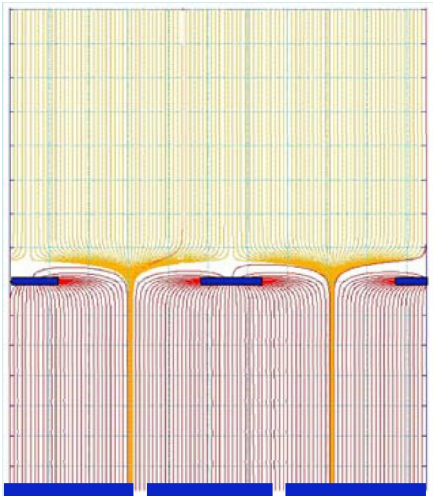




MPGD

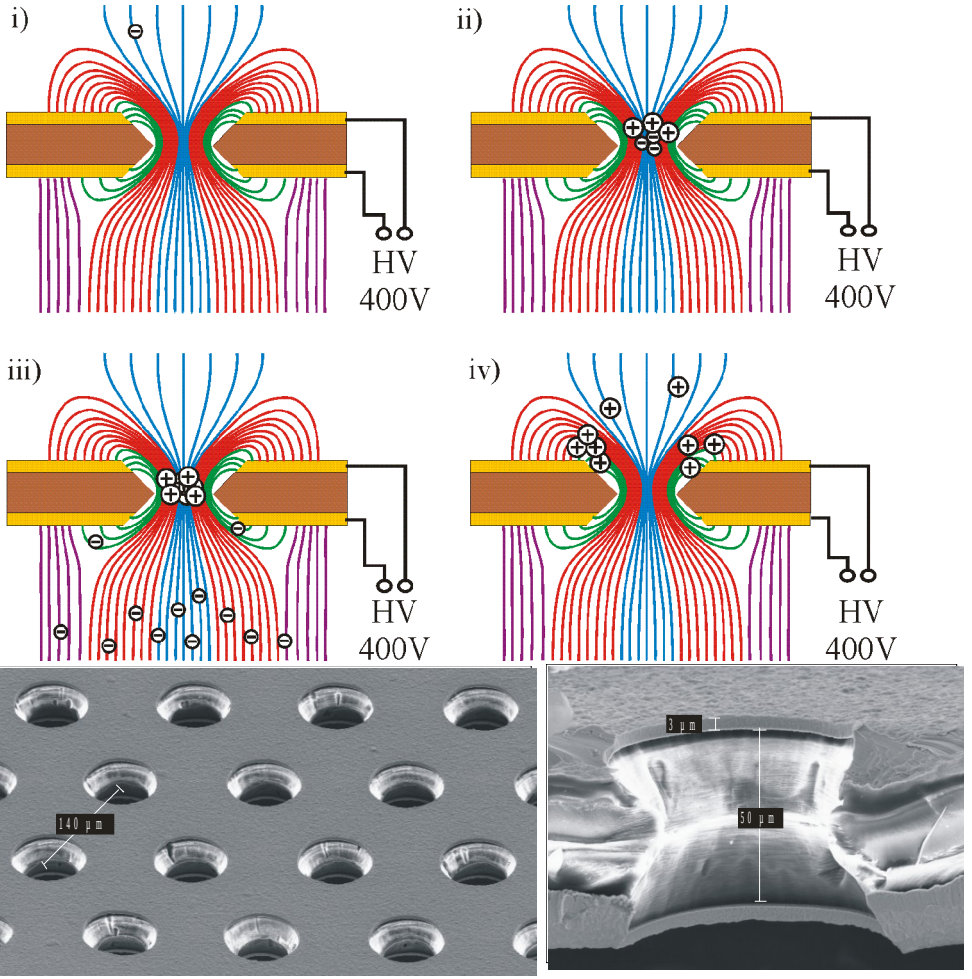
Micro-Mesh Gaseous Detectors



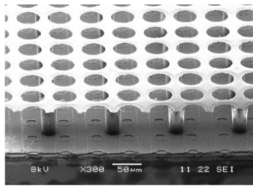


Y., Giomataris et al.,
Nucl. Instrum. Meth. A376:29-35,1996.

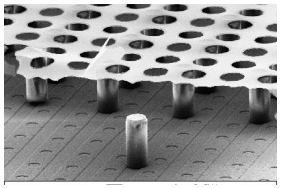
Gas Electron Multipliers



F. Sauli, Nucl. Instrum. Meth. A386:531-534,1997.



TPC + MPGD



- ion backflow can be reduced significantly
  => continuous readout might be possible
- small pitch of gas amplification regions (i.e. holes)
  => strong reduction of E×B-effects
- no preference in direction (as with wires)
  => all 2 dim. readout geometries can be used
- no ion tail => very fast signal (O(10 ns))
  => good timing and double track resolution
- no induced signal, but direct e^--collection
  => small transverse width => good double track resolution

Standard charge collection: Pads of several mm²

Long strips (l~10 cm, pitch ~200 µm)

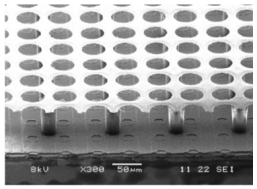
Could the spatial resolution of single electrons be improved?

$Ar:CO_2$ 70:30 → $D_t = 187\ \mu m/\sqrt{cm}$ → $\sigma = 21\ \mu m$

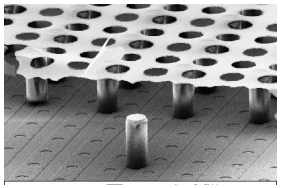
$Ar:CH_4$ 90:10 → $D_t = 208\ \mu m/\sqrt{cm}$ → $\sigma = 24\ \mu m$

Ar:iButan 95:5 → $D_t = 211\ \mu m/\sqrt{cm}$ → $\sigma = 24\ \mu m$

Smaller pads/pixels could result in better resolution!

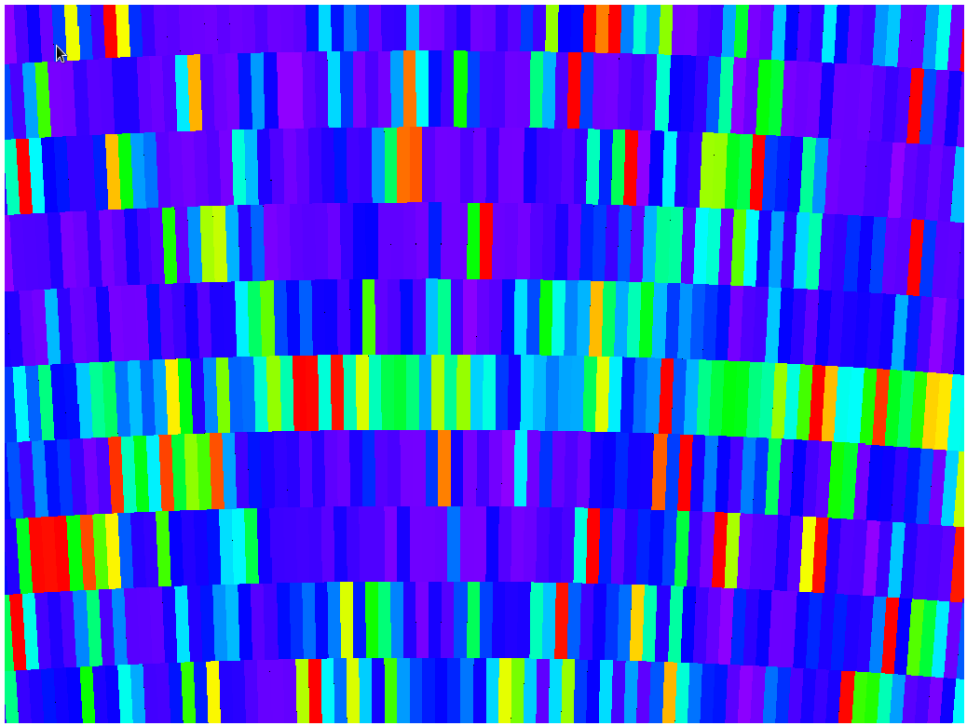


Highly pixelized Readout

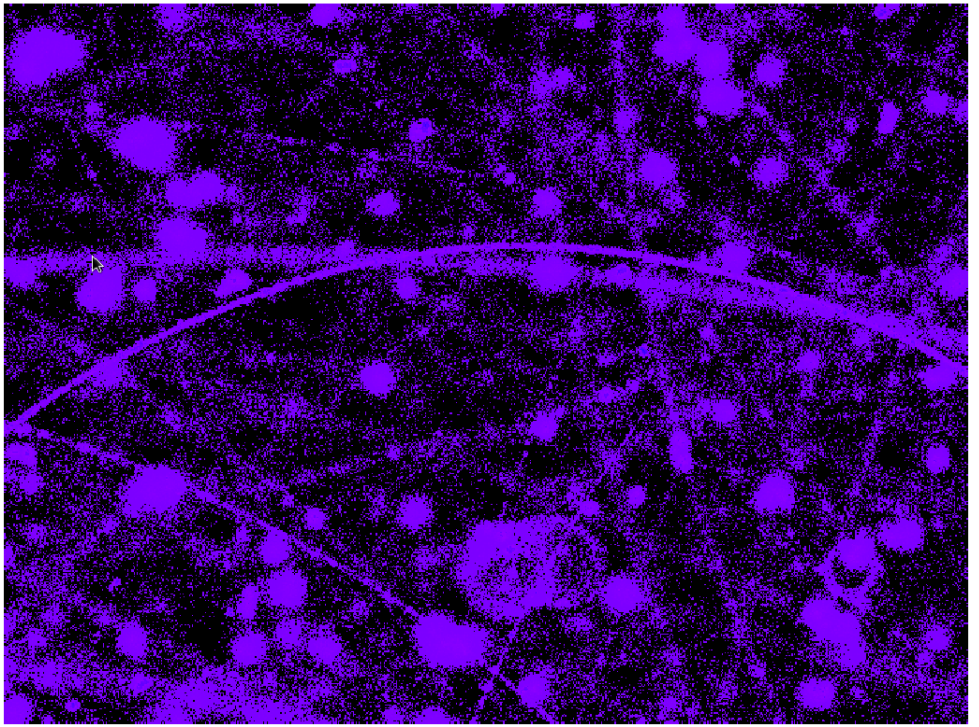


Simulation for the CLIC detector: M. Killenberg

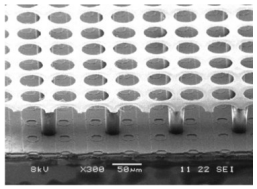
1×6 mm^2 pads



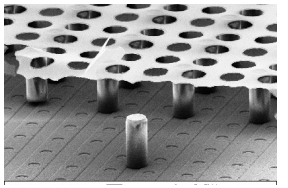
100×100 µm^2 pixels



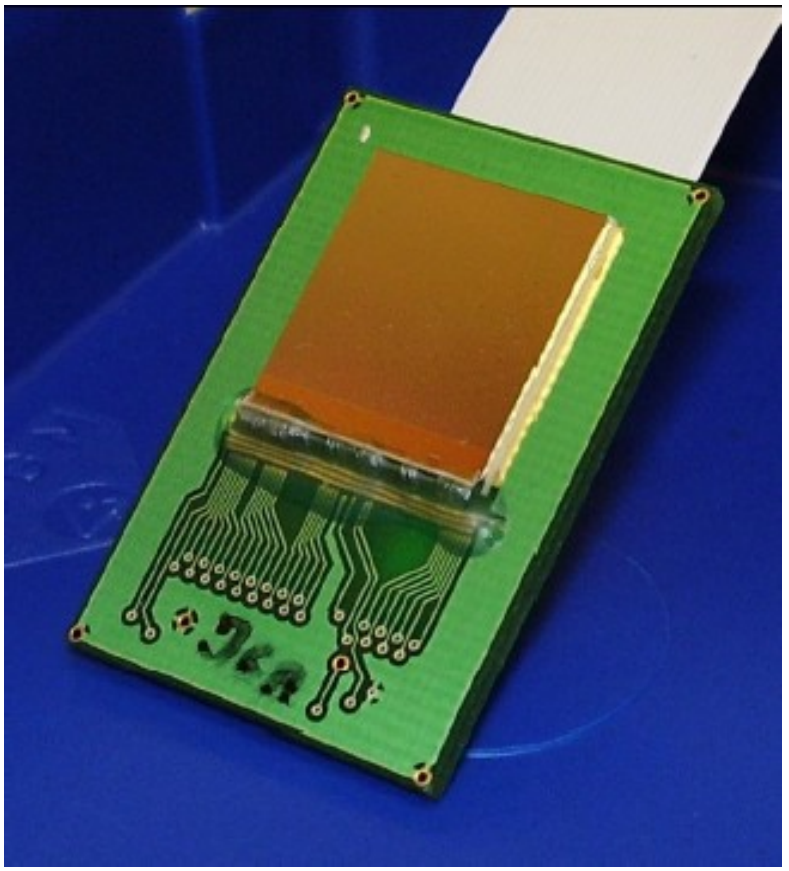
- Lower occupancy → better track finding
- Identification and removal of δ-rays and kink removal
- Improved dE/dx, because of primary electron counting
- Pad plane and readout electronics fully integrated



Timepix Chip



Timepix chip (1st version) derived from MediPix-2



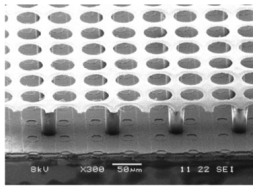
Available for tests since Nov. 2006

Number of pixel: 256 × 256 pixel
Pixel pitch: 55 × 55 µm²
Chip dimensions: 1.4 × 1.4 cm²
ENC: ~ 90 e^-

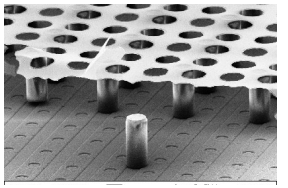
Each pixel can be set to one of these modes:

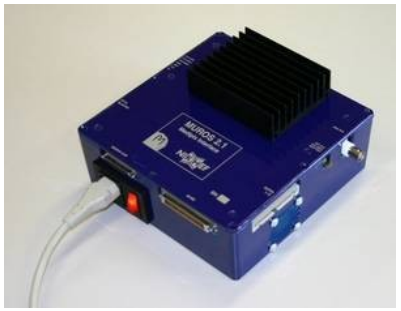
- Hit counting
- TOT = time over threshold
  gives integrated charge
- Time between hit and shutter end
- Hit/no-hit

Limitations: no multi-hit capability, charge and time measurement not possible for one pixel



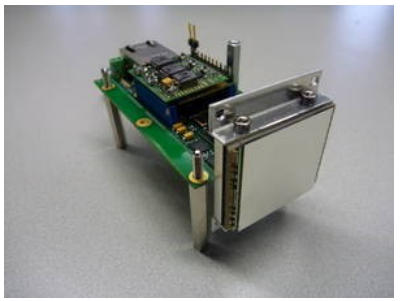
Readout Electronics





MUROS 2.1 designed at NIKHEF - still in wide use today, but not in production anymore,
can handle up to 8 chips, needs outdated NI card

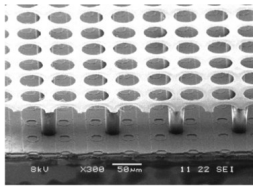
USB interface designed by TU Prague
very easy to handle/transport
but limited speed and functionality



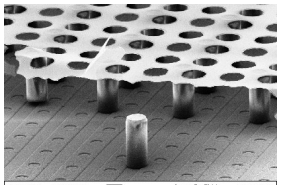
ReLaXd designed at NIKHEF – fast readout for 4 Medipix/Timepix chips

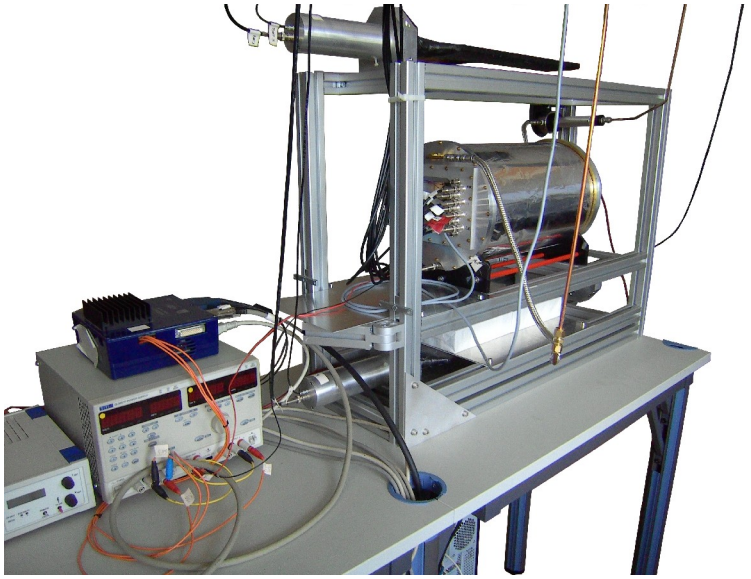
FITPix improved version of the USB-interface designed by TU Prague
can handle up to 16 detectors

Most systems are operated by the Pixelman software developed at the TU Prague.

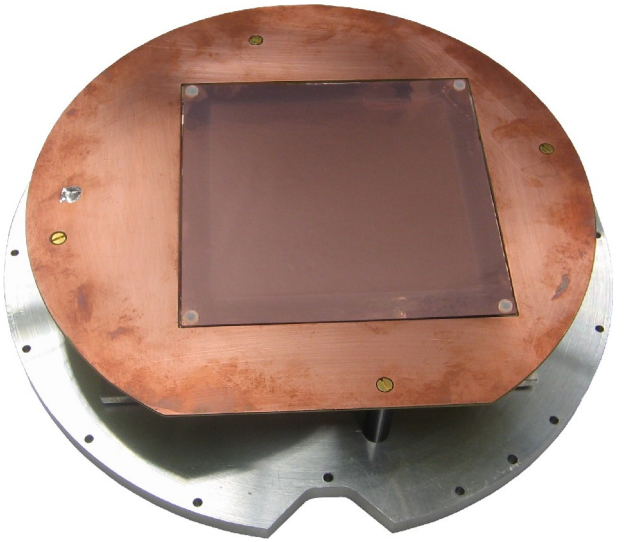


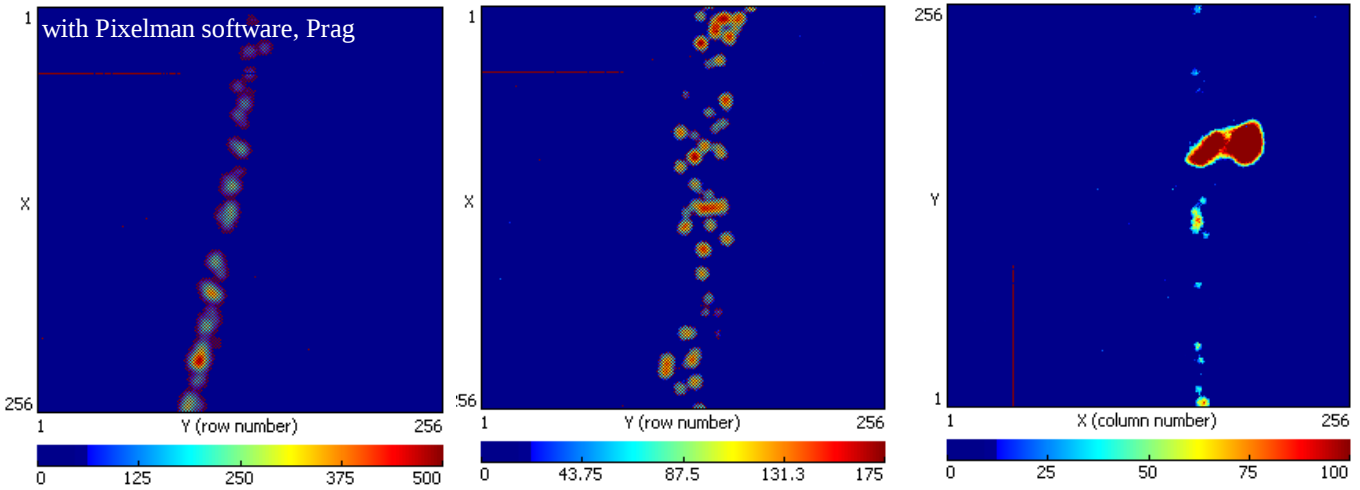
GEMs with Pixelized Readout

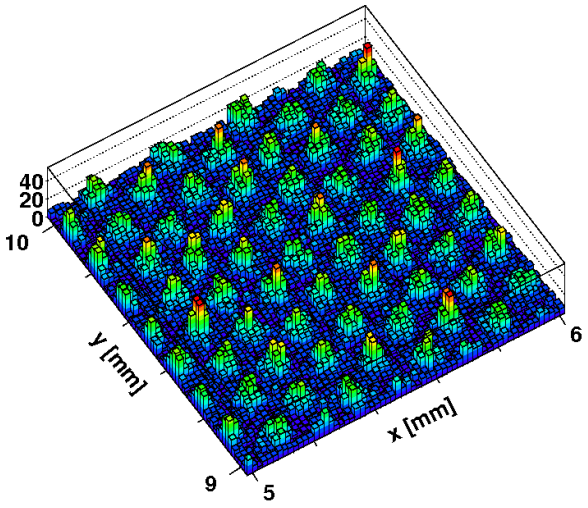


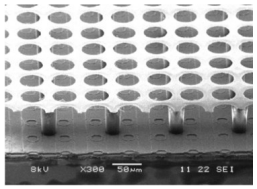


Prototype at Bonn
Drift length: 26 cm
Gas Amplification:
Stack of 3 standard CERN GEMs
1 Timepix chip
Gas mixture:
$He:CO_2$ 70:30

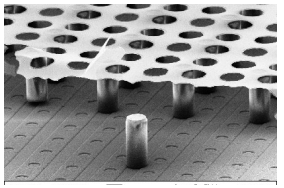


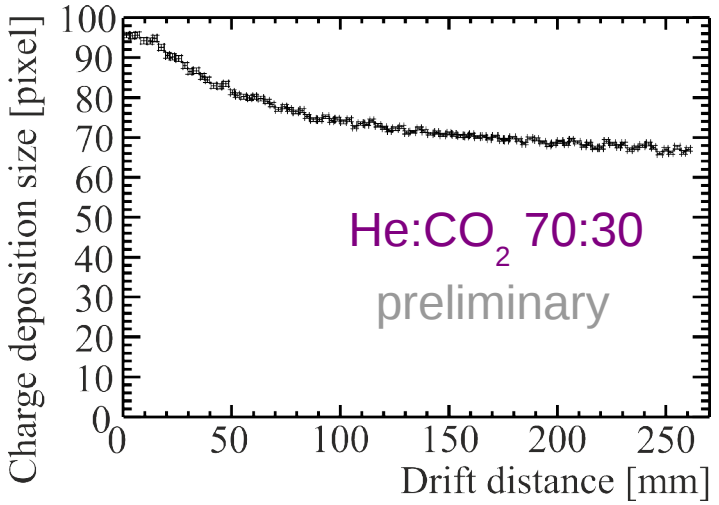


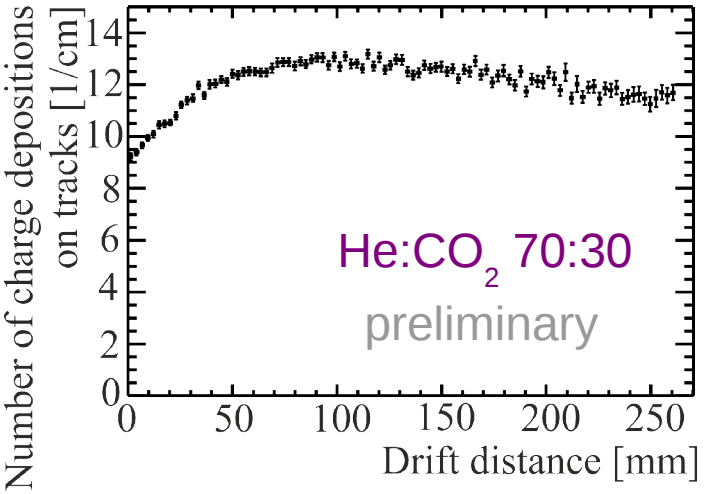


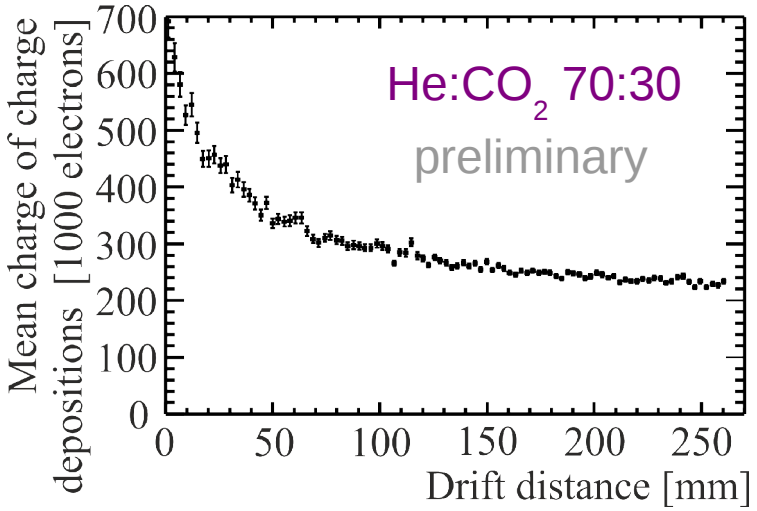


Properties of Charge Depositions

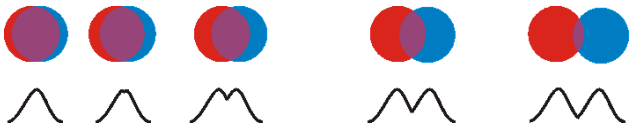




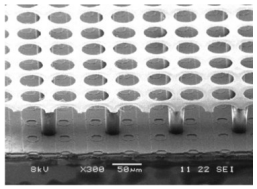




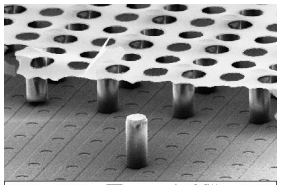
Charge depositions can be separated with higher probability after longer drift (better separated by diffusion).

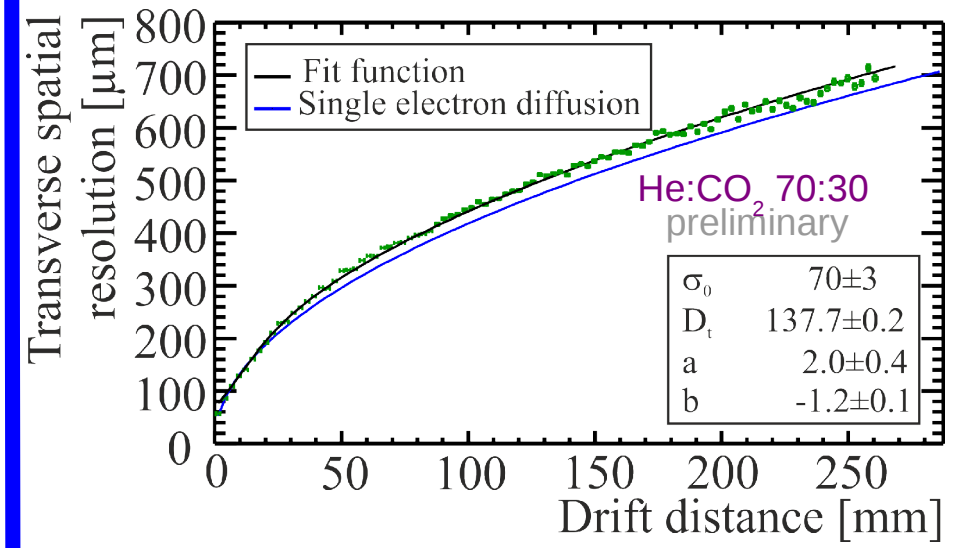


Gas gain of about 200,000 was used.
Charge depositions cover >65 pixels.



Spatial Resolution





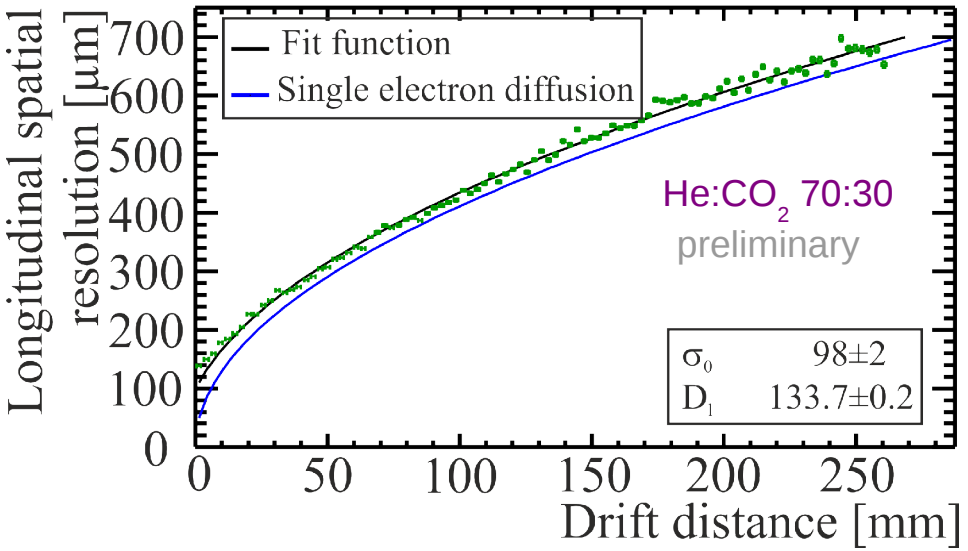
Spatial resolution of single electrons should increase with $\sigma = D_t\sqrt{z}$

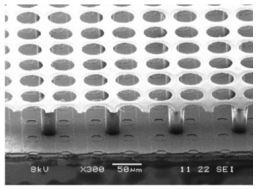
Due to limited separation power at short drift distances, one charge deposition may result from several electrons: $n = 1 + a\, e^{b}$

$\Rightarrow \sigma = \sqrt{\sigma_0^2 + D_t^2 z/(1 + a\, e^{bz})}$

Longitudinal spatial resolution is also close to the diffusion limit: $\sigma = D_l\sqrt{z}$

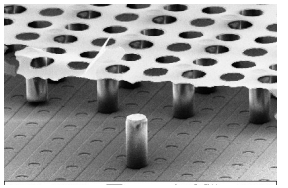
Similar good performance was observed in high magnetic fields up to B = 4 T.



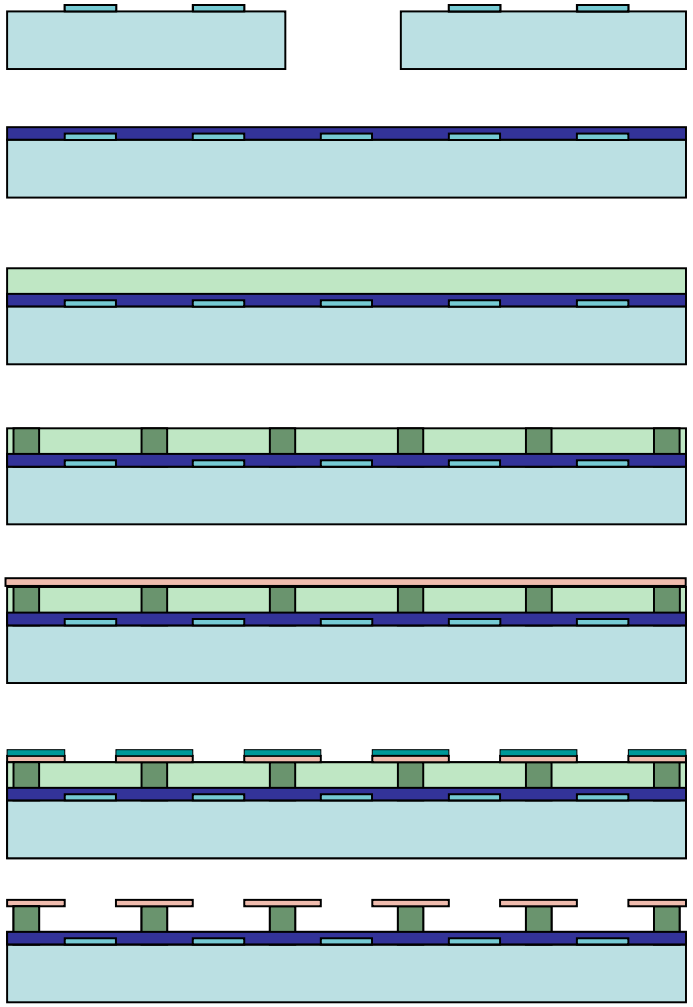


Production of InGrids

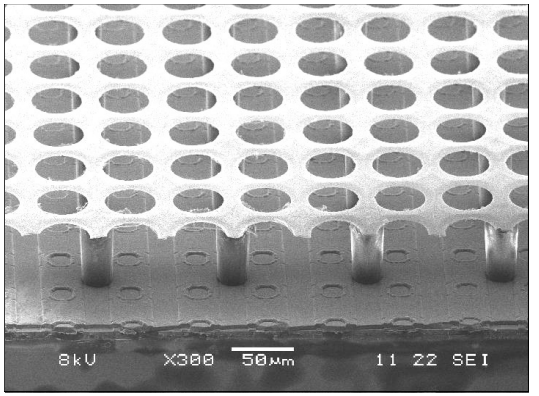
MESA+ Institute for Nanotechnology

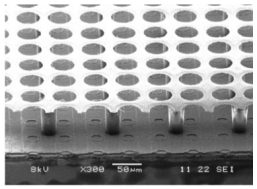


The production of InGrids was pioneered by the University of Twente/MESA+.

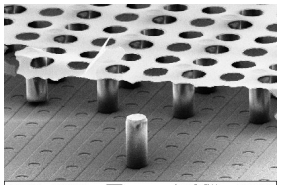


1. Dicing of Wafer
2. Formation of Si_xN_y protection layer
3. Deposition of SU-8
4. Pillars-like structure formation
5. Deposition of thin Al layer
6. Formation of Al grid
7. Development of SU-8

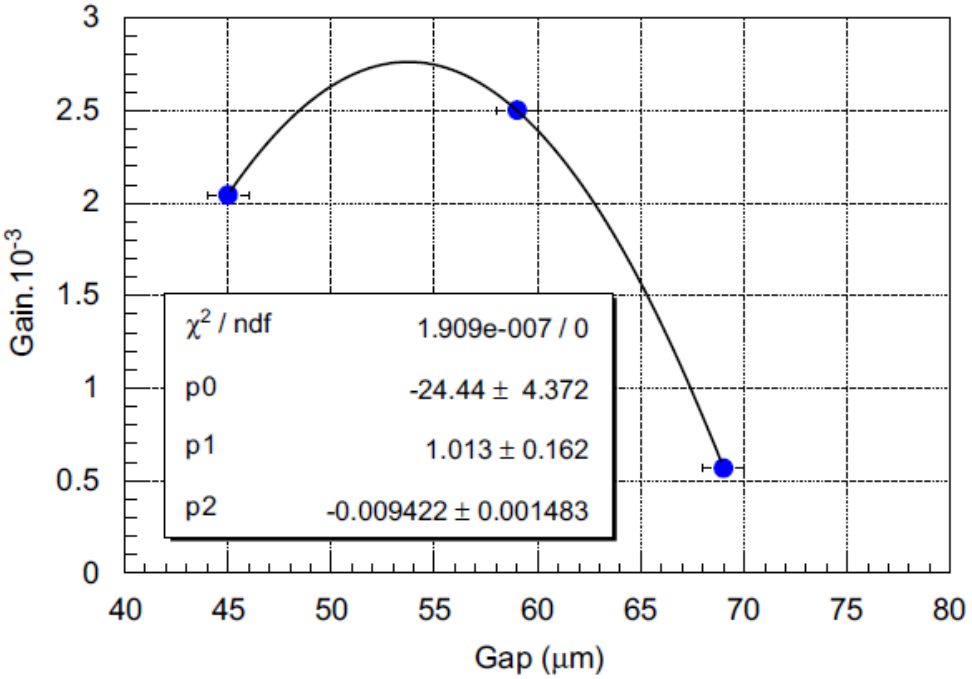




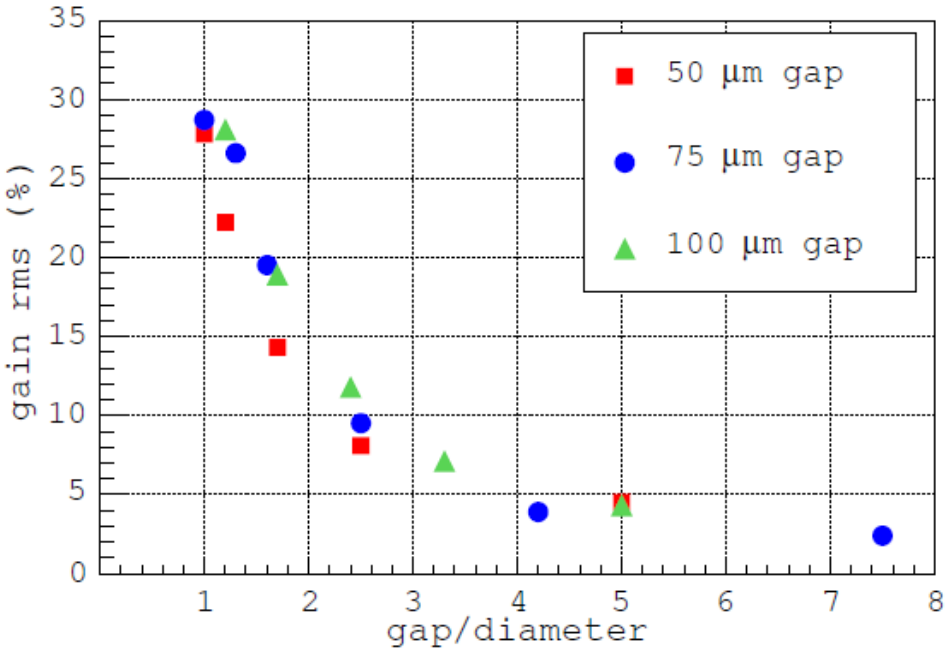
Optimization of InGrids



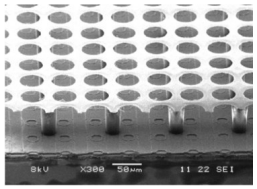
Detailed studies have been performed to optimize the layout of the structure.
(NIMA 591, pp. 147, 2008, PhD. Thesis of M. Chefdeville, NIKHEF)



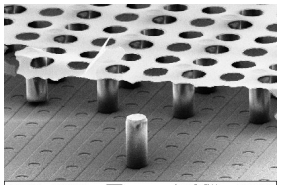
The influence of the gap size and hole diameters on gain, energy resolution, ion feedback and collection efficiency were measured.



Also the layout of the supporting structures (pillars and dykes) was optimized to give the highest mechanical strength.

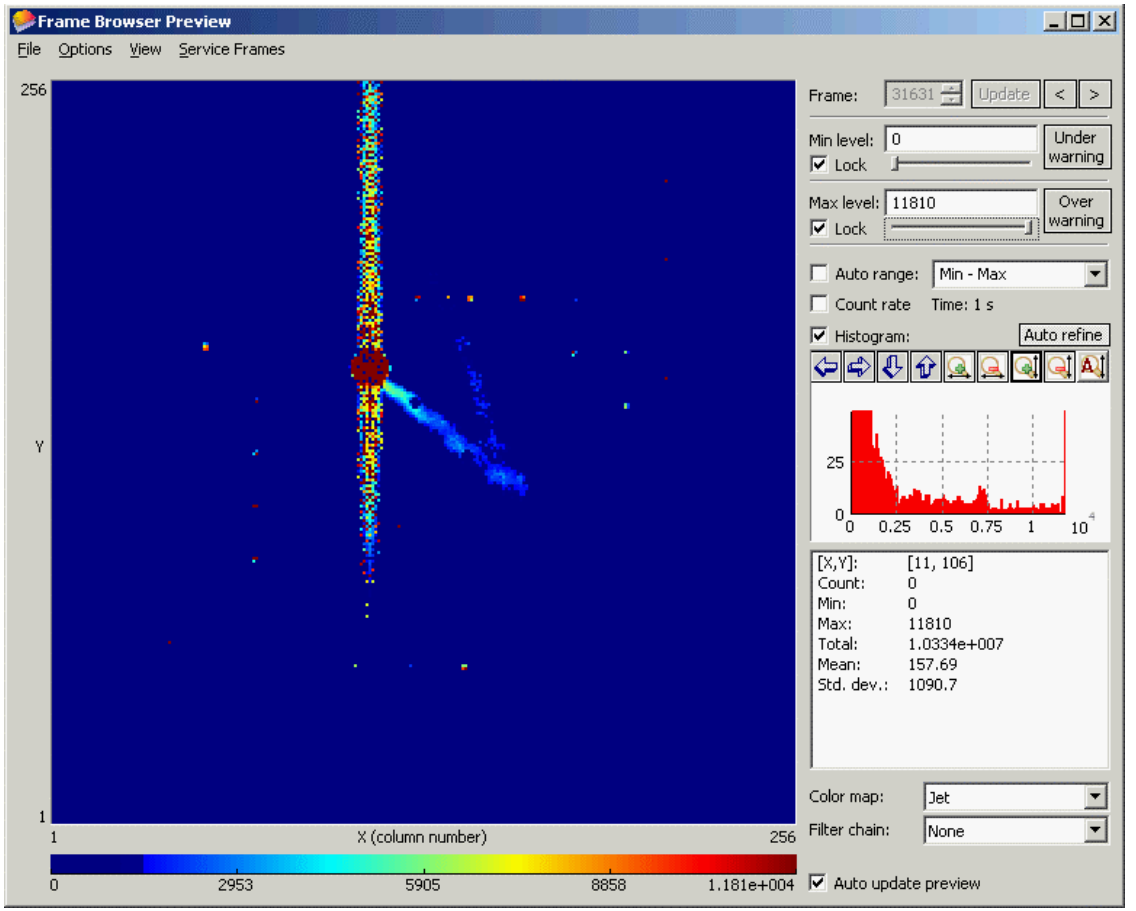


Protection Layer



Discharge triggered for example by highly ionizing particles could easily destroy the the chip. The charge collected by one pixel was too high.

A protection layer is placed on the chip to disperse the charge on many pixels and thus lower the input current per pixels. Besides, the charge is removed slowly and thus quenches the discharge.

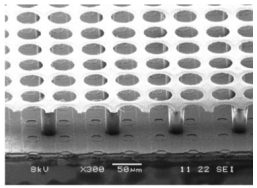


<u>high resistive material</u>

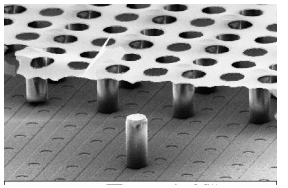
15 µm aSi:H (~10^{11} Ω·cm)

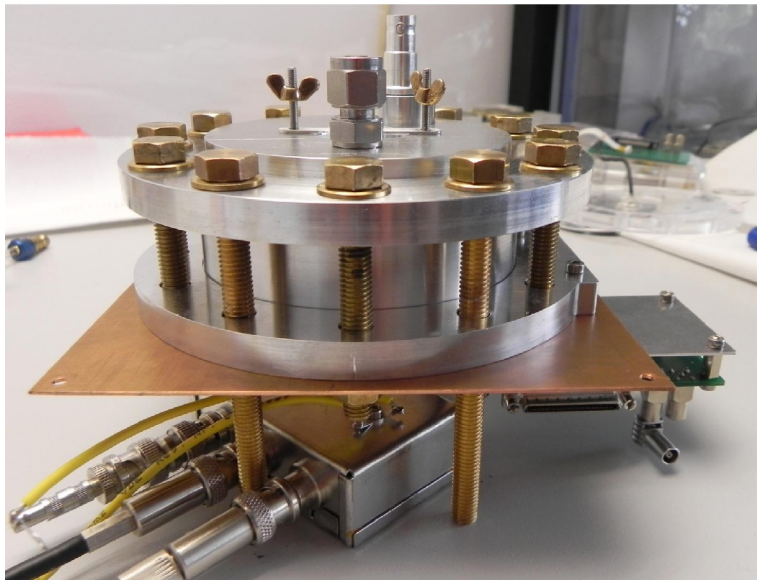
8 µm Si_XN_Y (~10^{14} Ω·cm)

Chips survives several thousand discharges triggered by αs.

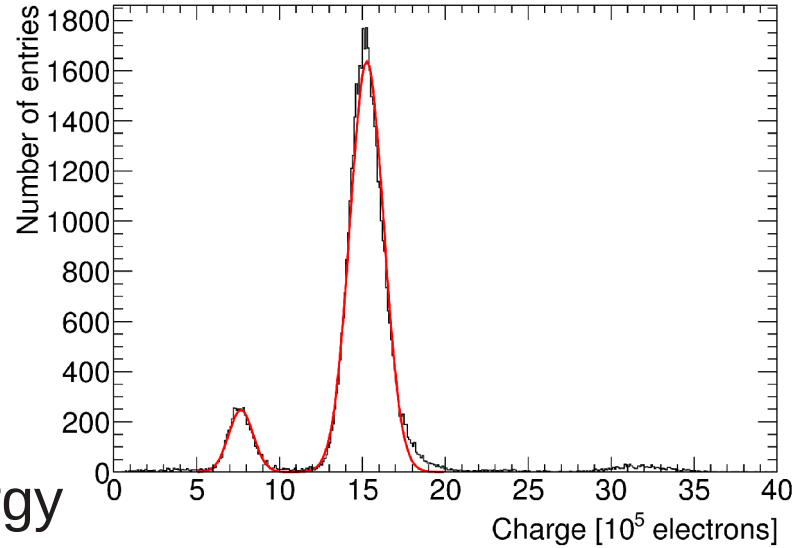


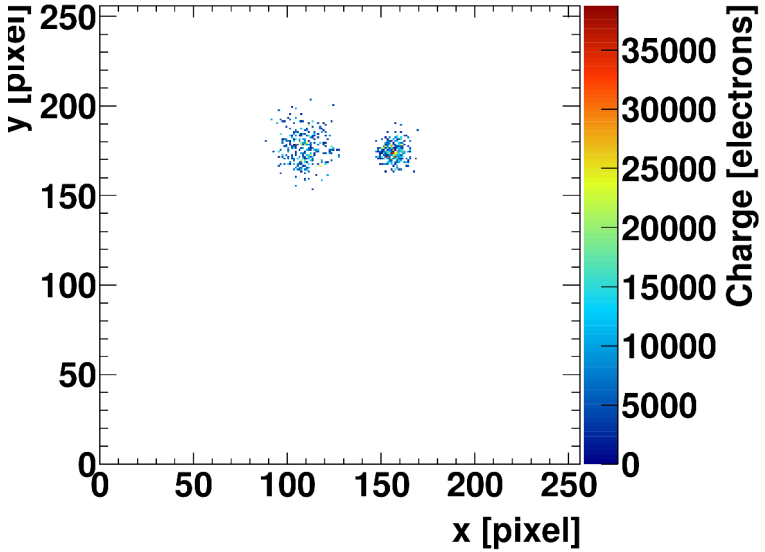
Energy Resolution

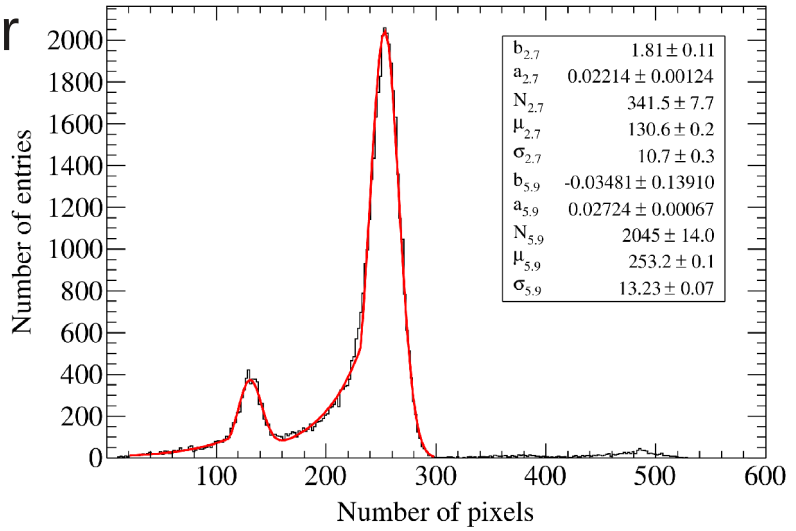


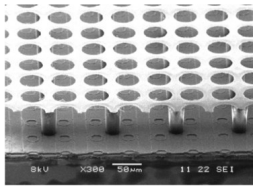


Test with ^{55}Fe source show excellent energy resolution.
In particular for pixel counting.

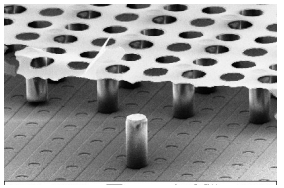




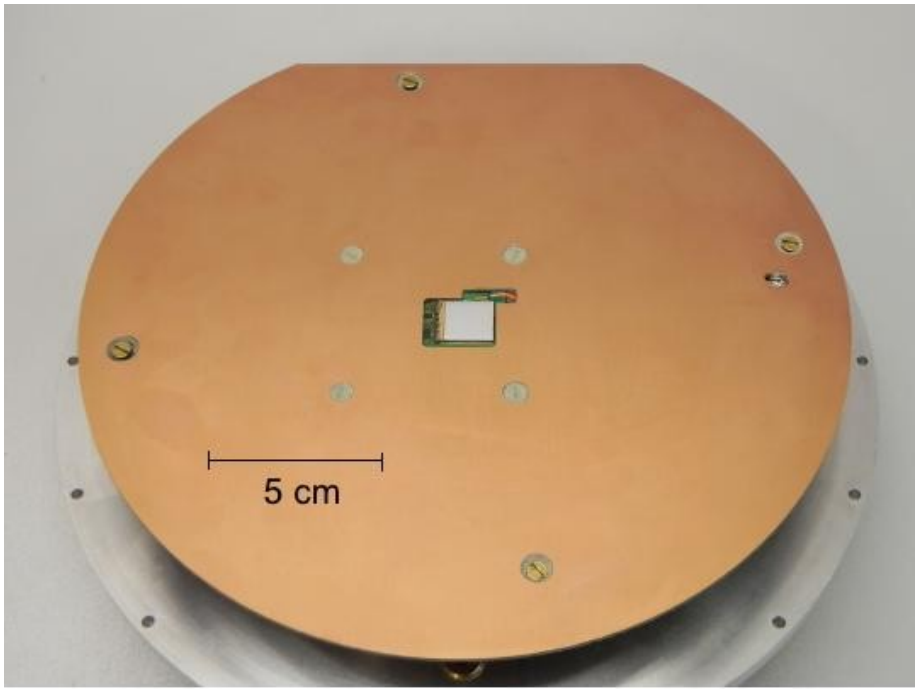


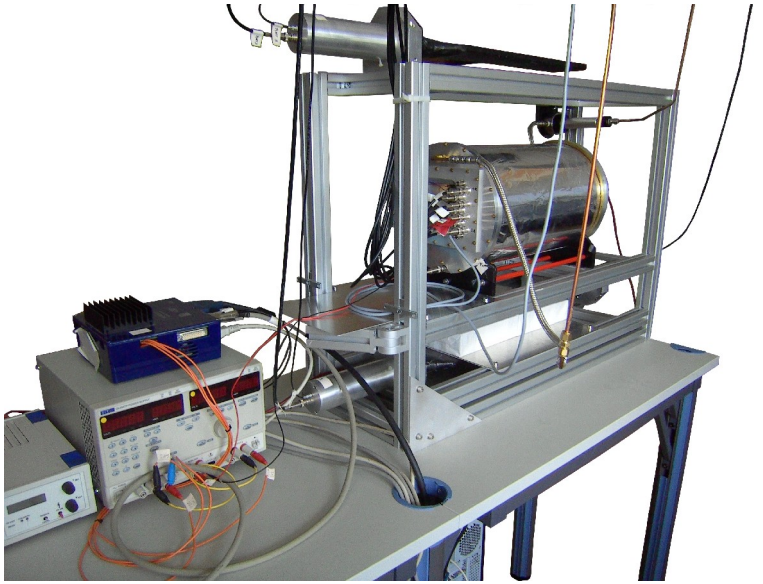


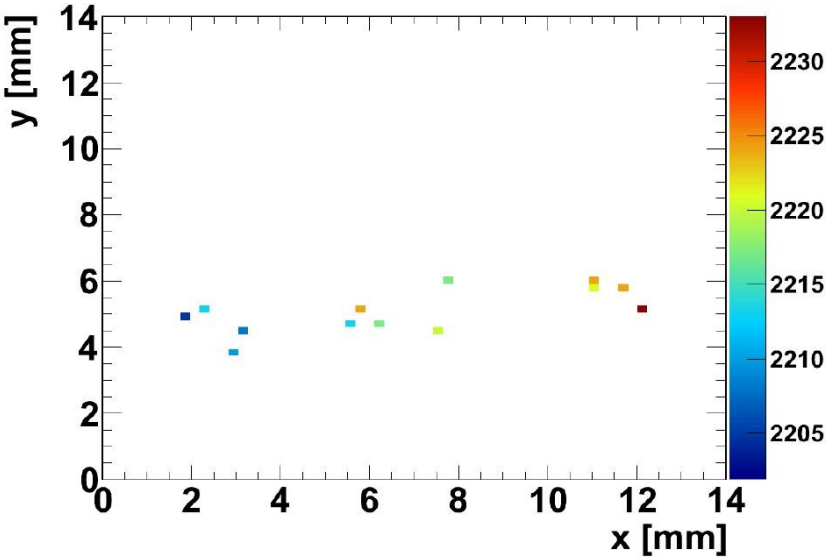
InGrids in a TPC

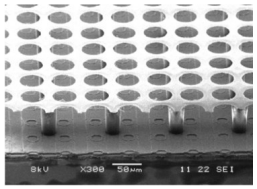


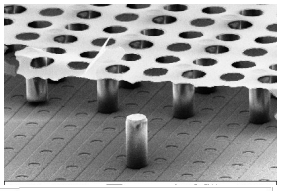
<u>Same setup as with GEMs:</u>
Max. drift length: 26 cm
Measures cosmic muons
Drift field: 450 V/cm
Gas: $He:CO_2$ (70:30)



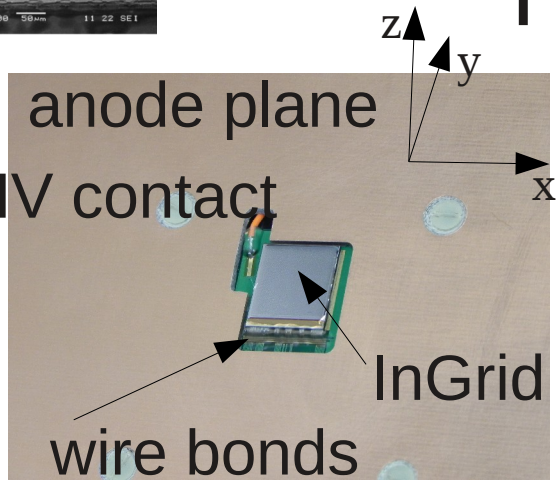






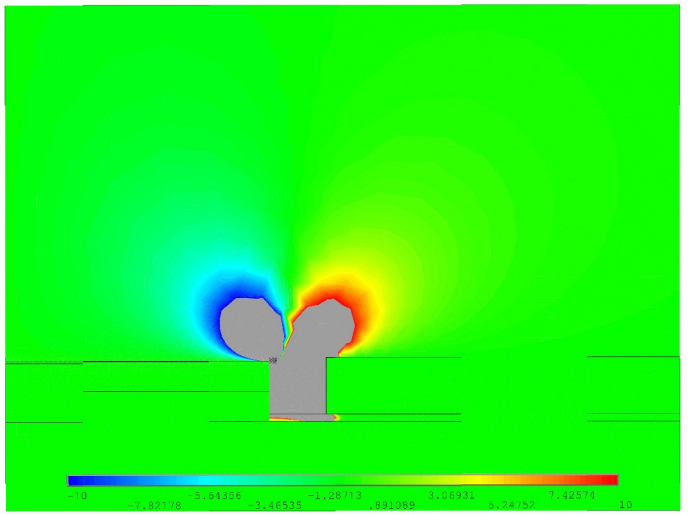


Field Distortions (I)

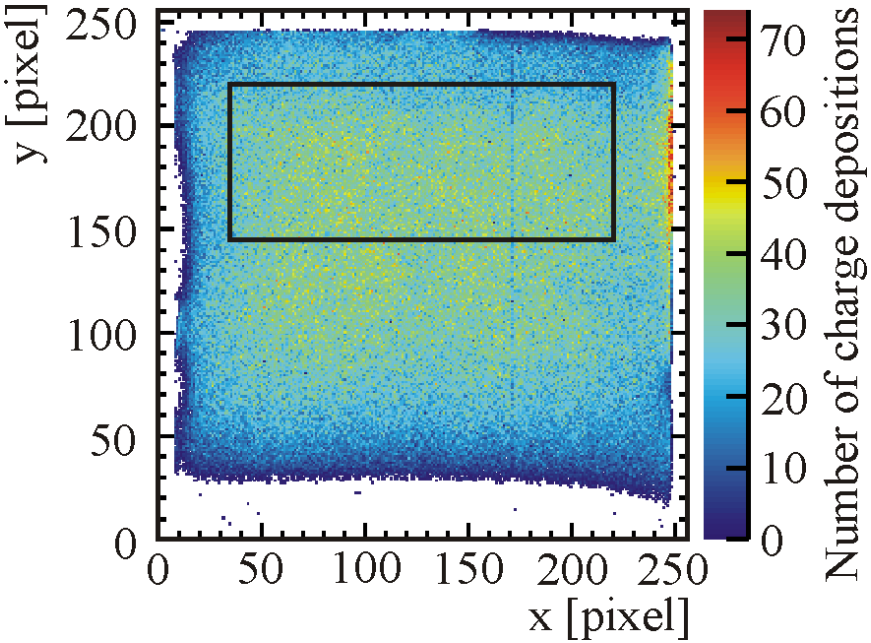


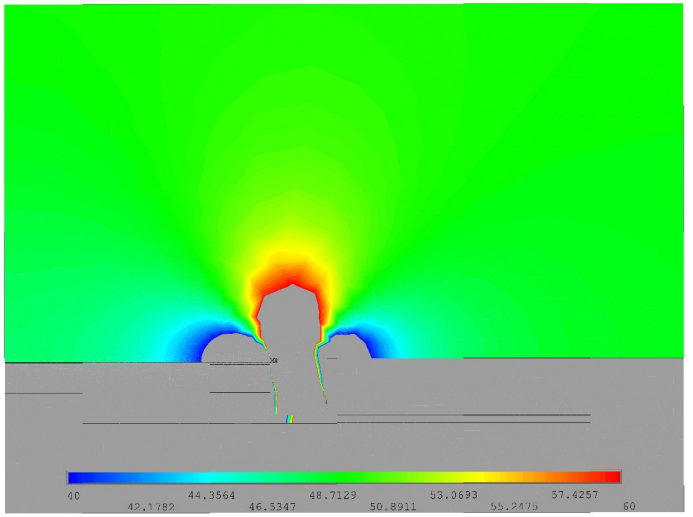
due to wire bonds and space between grid and anode plane

=> Good area was chosen to indicate best performance

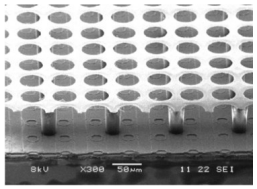


Electrical field in x-direction V/cm

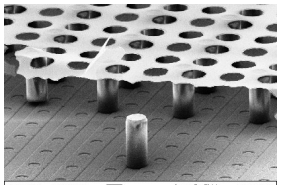


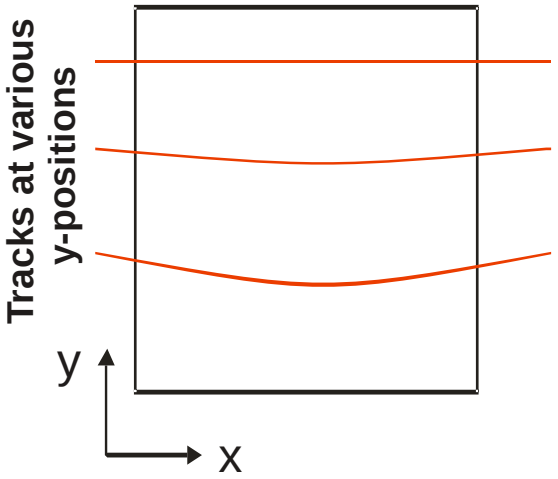


Electrical field in z-direction V/cm

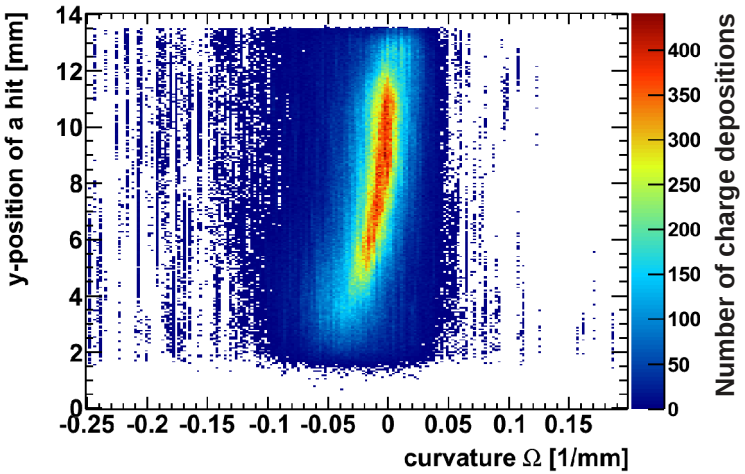


Field Distortions (II)



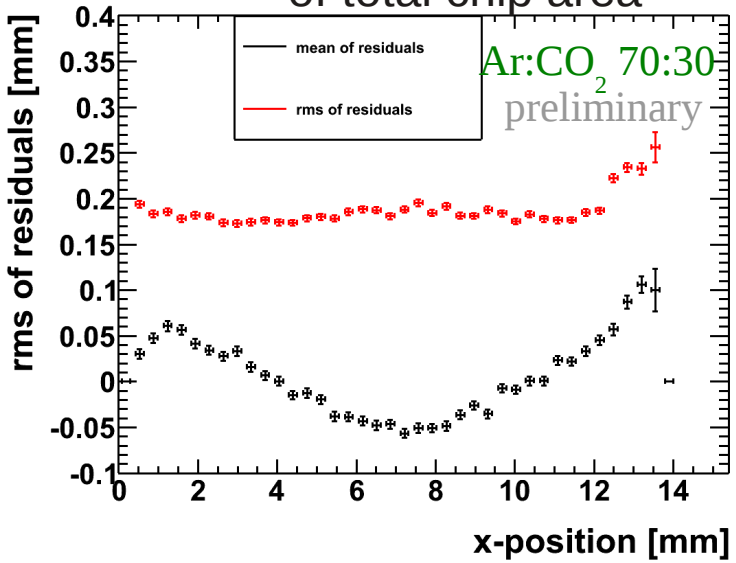


Field distortions generate an artificial curvature of tracks. Approximated by helix to determine good area.

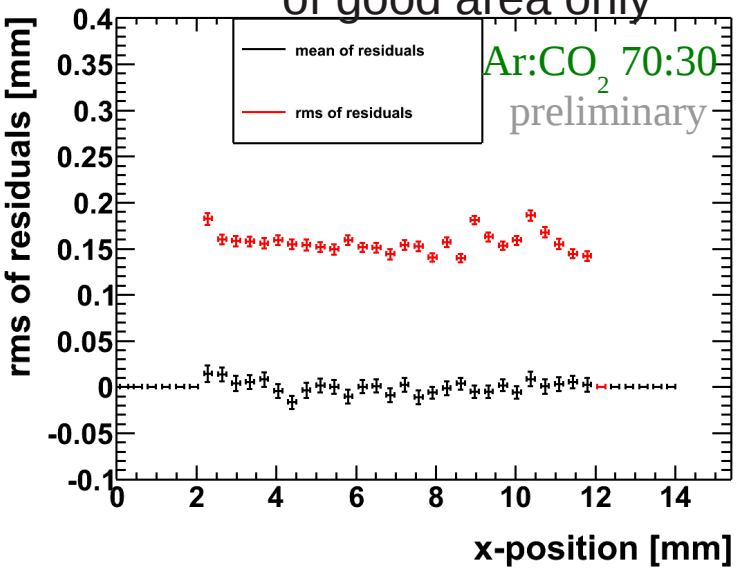


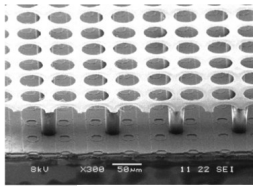
Properties of residuals

of total chip area

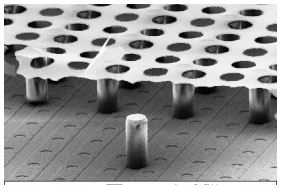


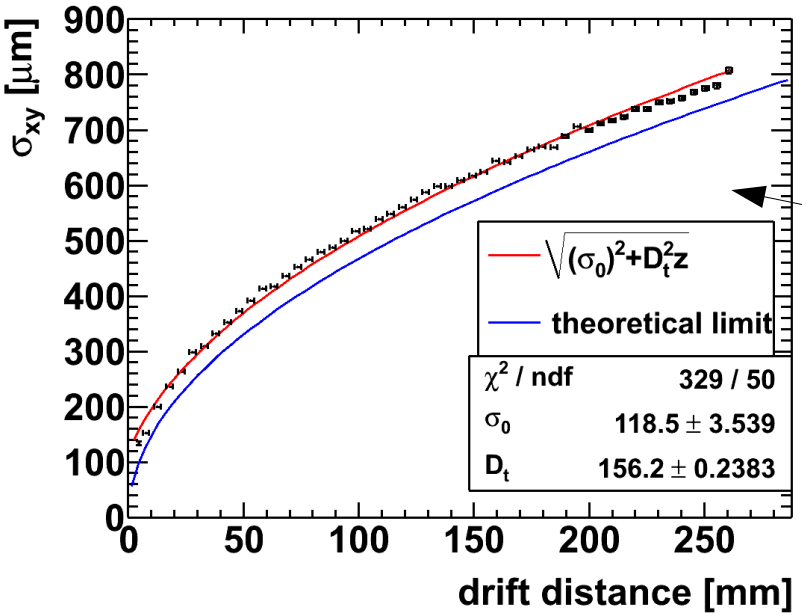
of good area only



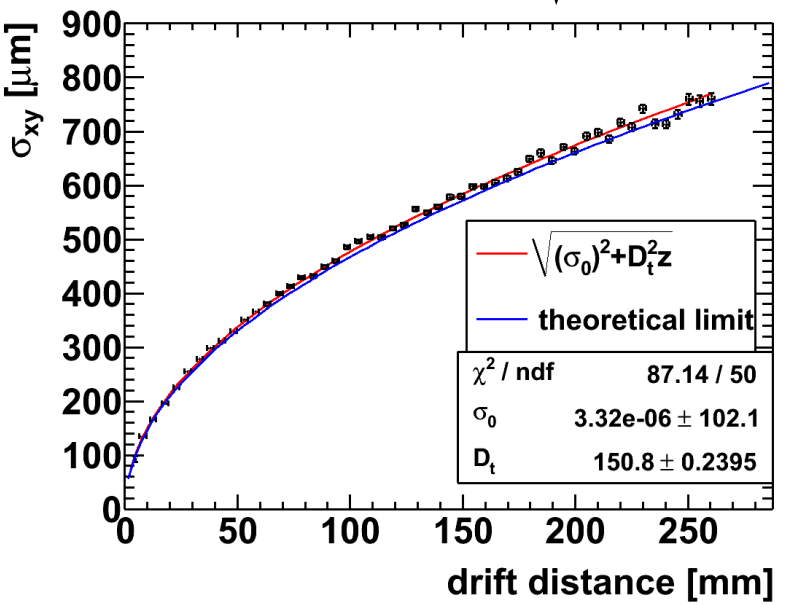


Spatial Resolution





Spatial Resolution on the complete chip and on the good area only.

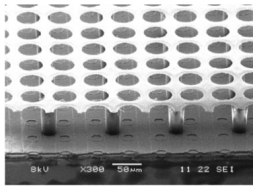


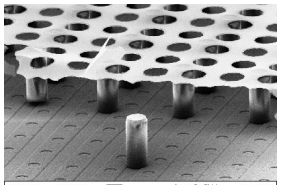
Transverse spatial resolution right on diffusion limit of single electrons.

Theoretical limit:

$\sigma = D_t\sqrt{z}$

with diffusion coefficient D_t calculated with Magboltz.

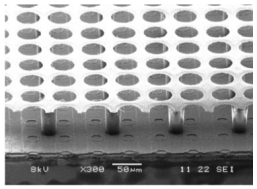




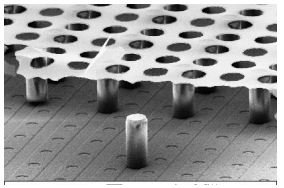
Principle of a highly pixelized readout has been demonstrated successfully!

But what is missing for application in particle physics experiments?

1. Better chip → Timepix-3
2. Mass production of InGrids → Production at IZM
3. Adapted readout system → SRS system
4. Deal with field distortions
5. Cooling



Application LCTPC

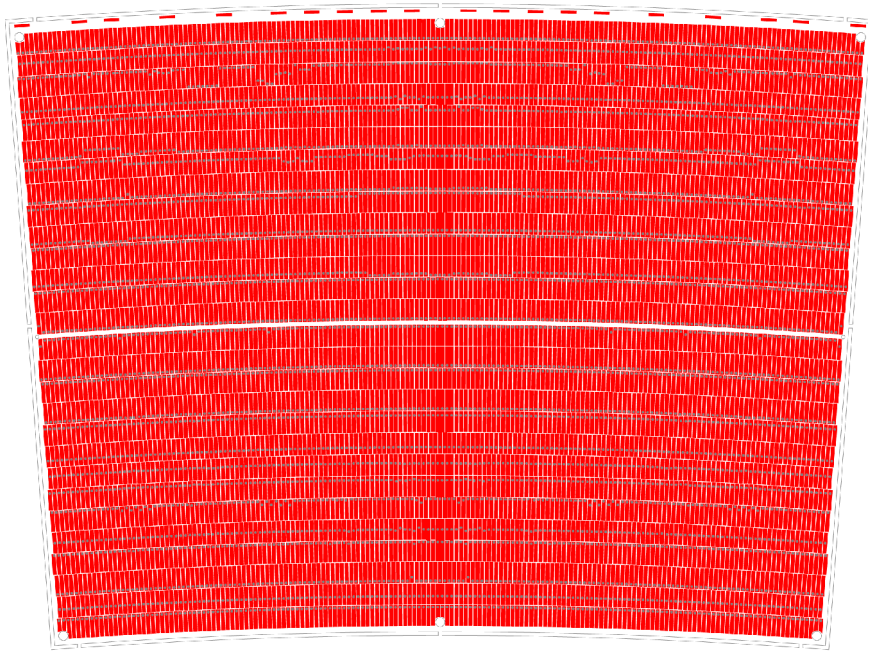


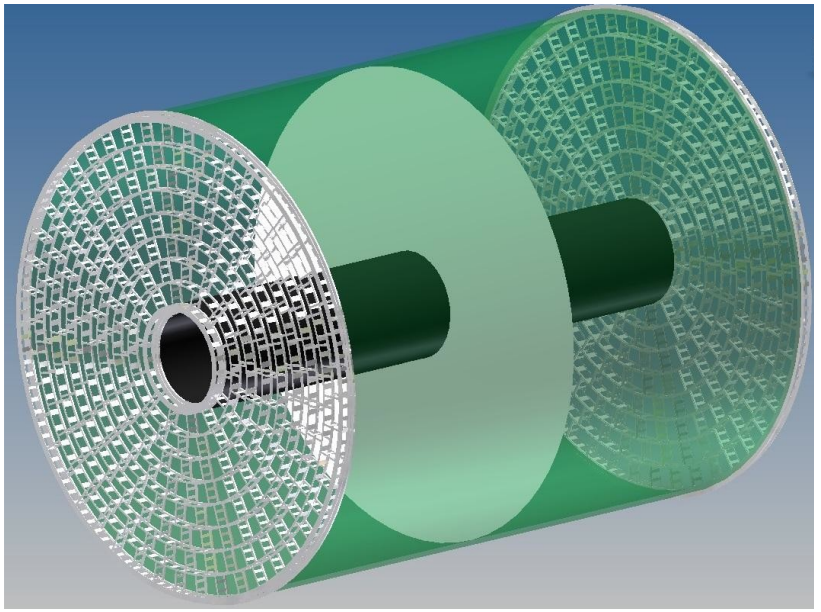
One of the two detector concepts at ILC foresees a large TPC as a central tracking device. Micropattern gas amplification stages are needed to fulfill requirements.

size of endcaps ~10 m^2

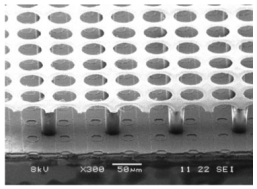
8 rows of MPGD detector modules;
module size ~17×23 cm^2

240 modules per endcap

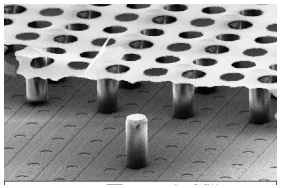




To readout the ILD-TPC with InGrids, one needs ~100-120 chips per module
→ 25000-30000 per endcap



Timepix-3



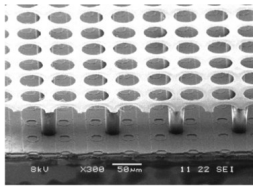
Layout has basically been finished.
Specs see table (from:
Timepix3 Designer Manual v1.0)

Some simulations are still ongoing. chip will be submitted in a few weeks.

Most importantly:
- Charge and time will be available
  - For every pixel,
- Multi-hit capable
- Very high output rate: 8×640 MHz
- Time resolution of 1.5 ns

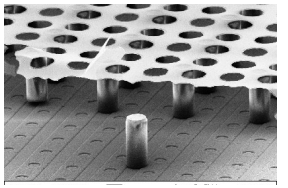
General Requirements	
Pixel size	55 µm x 55 µm
Pixel matrix array	256 x 256
Target floorplan	3 sides buttable and minimum periphery
Highly Configurable	HEP platform for many projects
Time stamp and TOT recorded simultaneously	YES
No event counting mode	Only for testing
Technology	IBM 130nm DM 4-1
Power consumption	<1.5W/cm^2 (~45 µW/pixel) @1.2 V
TSVs possibility	YES
Chip Readout Modes	
Data-driven readout (token pass)	YES
Zero-suppressed and Sparse data readout	YES
Dead time free	YES (if moderated count rate)
Time Stamp	
Global Time stamp (bunchID)	40 MHz (25ns)
Global Time stamp range	14bits (409.6 µs)
Accurate Time stamp per pixel	4bits → 1.56ns resolution (640 MHz)
Local Oscillator frequency	640 MHz
On-pixel local oscillator tuning	Locked using periphery PLL
TOT	
TOT Clock reference	40 MHz (25ns)
TOT range	10 bits
Periphery	
Analog Blocks	Band-Gap, DACs and Test Pulse
E-fuses (chip ID, hard-wire configuration)	YES
Programmable PLL	40 → 40, 80, 160, 320, 640 MHz
Periphery/output clock	40, 80, 160, 320 MHz
RO architecture	[1 ... 8] LVDS DDR 8b/10b Encoding

universitätbonn

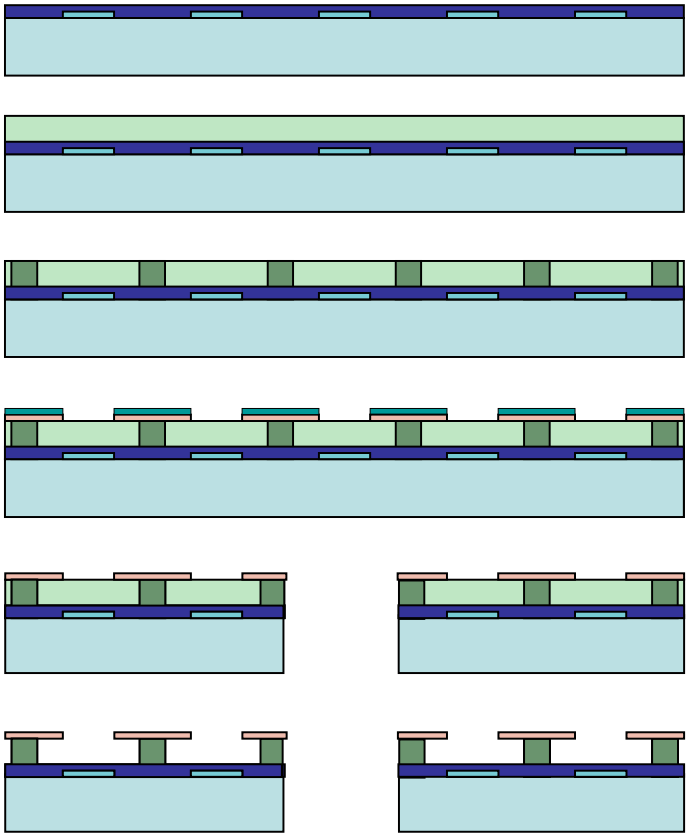


Wafer-based Production

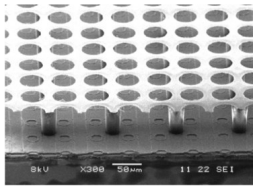
Fraunhofer IZM



Production at Twente was based on 1 - 9 chips process.
This could not satisfy the increasing demands of R&D projects.
New production set up at the Fraunhofer Institut IZM at Berlin.
This process is wafer-based → 1 wafer (107 chips) is processed at a time.

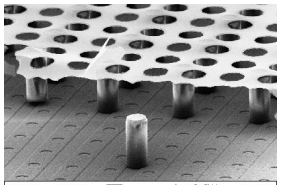


1. Formation of Si_xN_y protection layer
2. Deposition of SU-8
3. Pillar structure formation
4. Formation of Al grid
5. Dicing of Wafer
6. Development of SU-8



Wafer-based Production

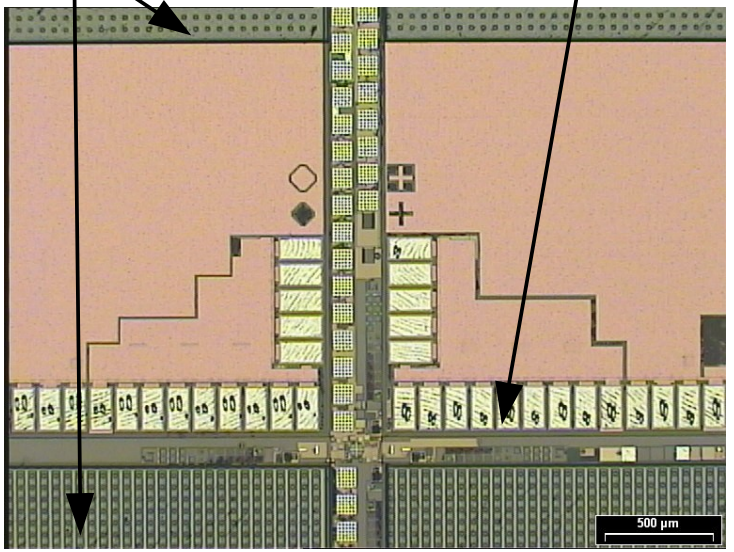
Fraunhofer IZM



Main challenges: - Formation of layers, in particular protection layer
- Deposition of Al
- Final development of SU-8 → still chip-based

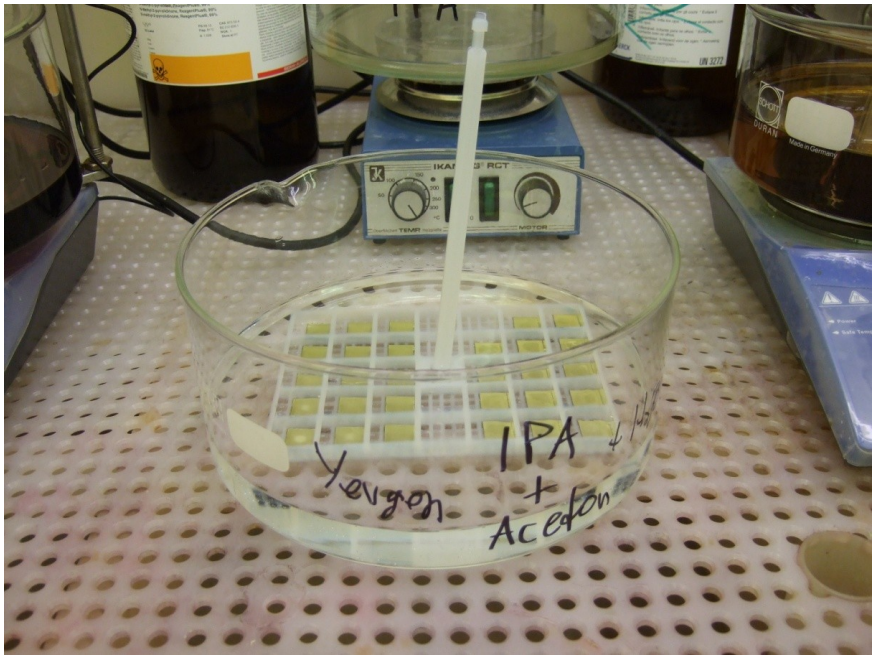
MESA+ Institute for Nanotechnology

SiRN should not cover bond pads

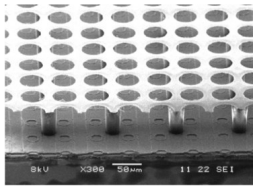


First tests: mechanical mask
→ failed due to thermal stress
Better: poyimide mask chem. removed

After development of pillars,
the grid is too fragile for dicing

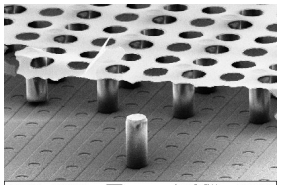


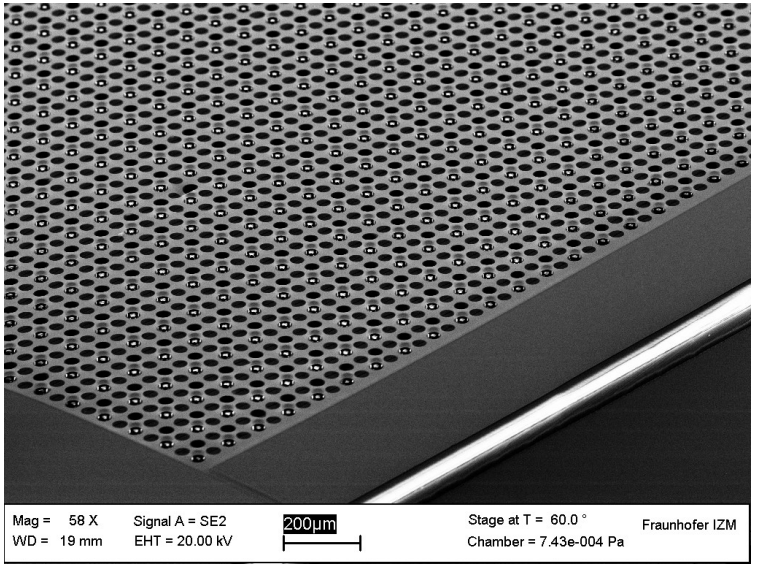
Time consuming

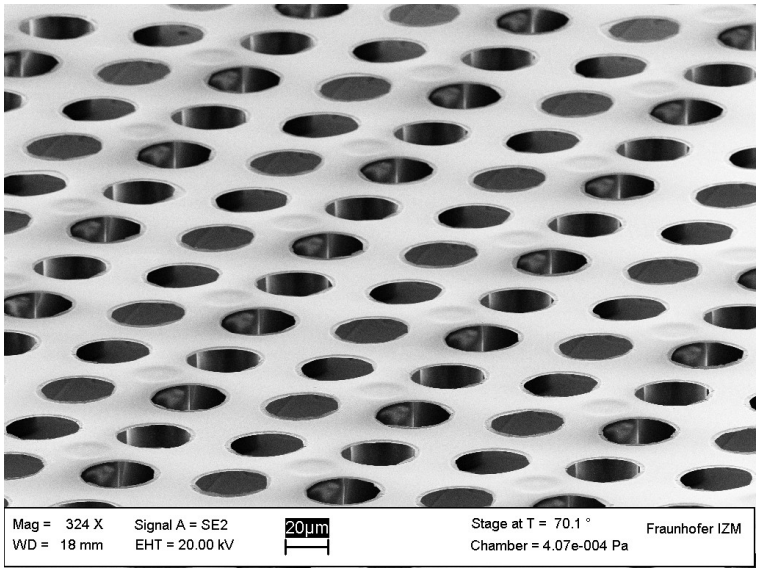


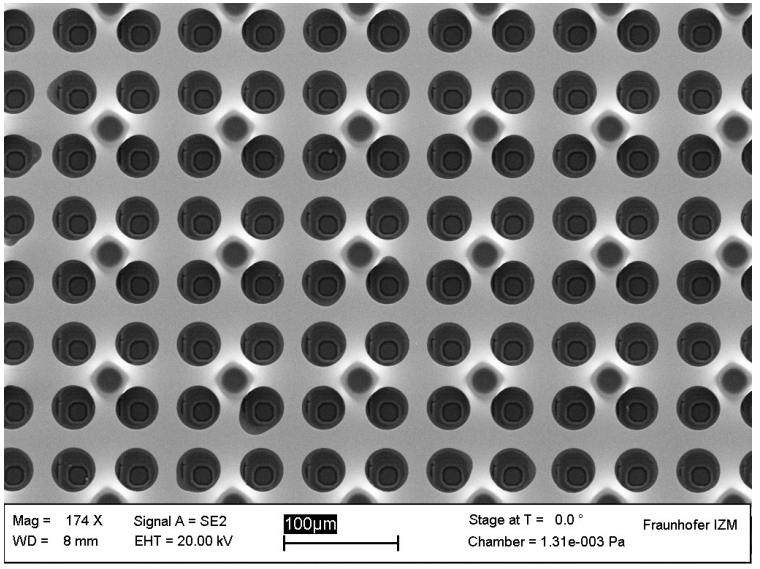
SEM Pictures

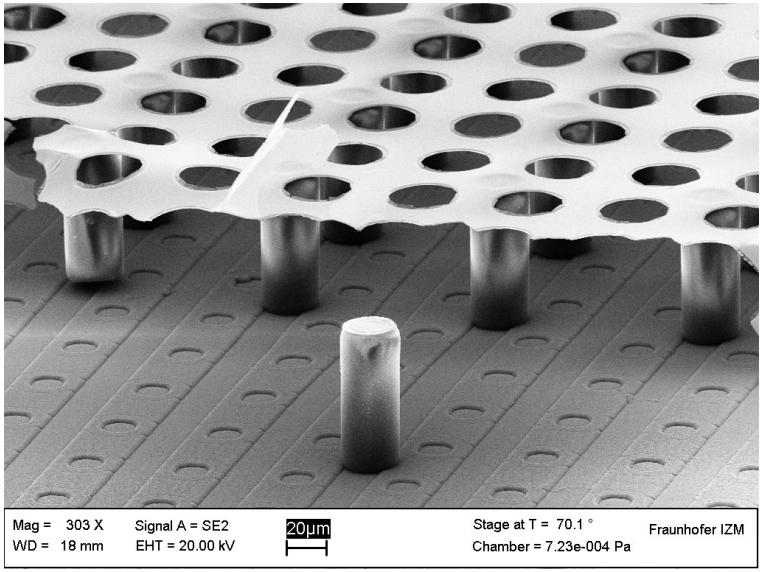
Fraunhofer IZM

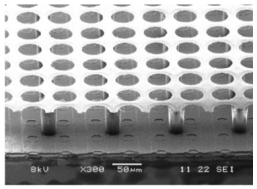




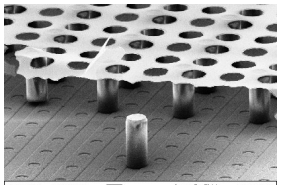








Production History



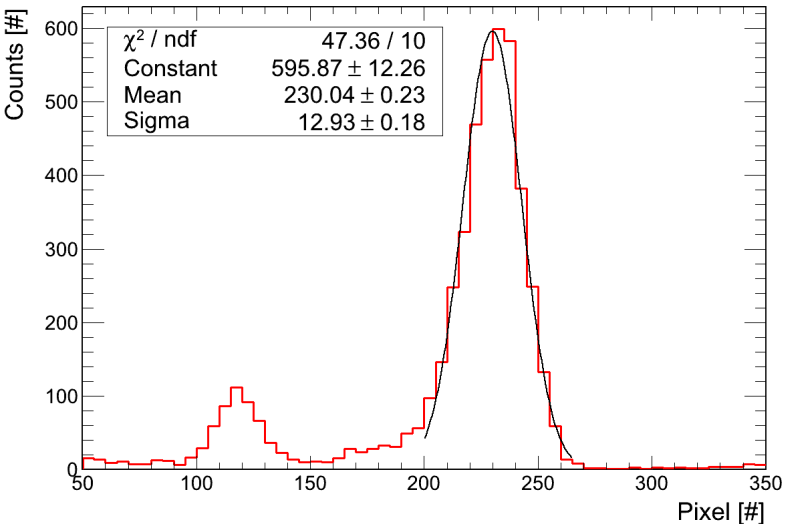
1. batch (10/2011): Problems with resistive layer and Al-grid
2. batch: InGrids worked well, good energy resolution (σ_E/E~7%)
   (12/2011) Resistive layer proved vulnerable (chips died after 2 weeks)
3. batch: Chips survived many thousand X-ray-induced sparks
   (9/2012) But 7 out of 10 chips died in a hadronic test beam at CERN
4. batch: 4 wafers with different resistive layer thicknesses (4 µm, 8 µm)
   (12/2012) Problems with the production (machine failure)
   → only few good chips
5. batch: in preparation
6. batch: planned (6 wafers)

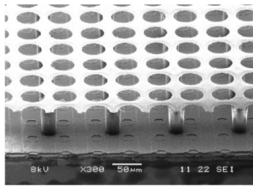
Energy resolution is similarly good as before:

σ_E/E=5.6 % for the pixel spectrum

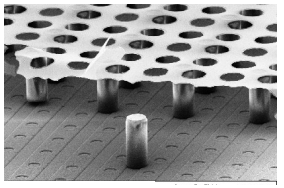
σ_E/E=7.2 % for charge spectrum

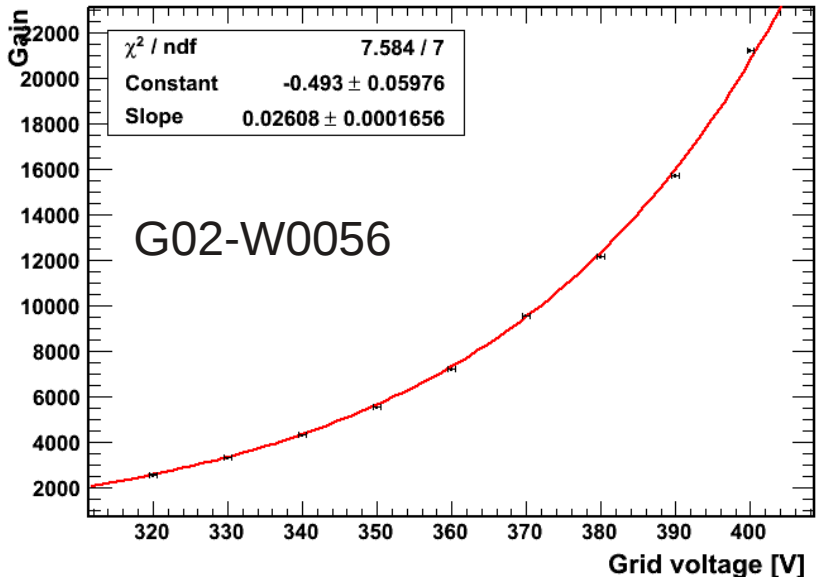
G02-W0056 (of 3. batch)

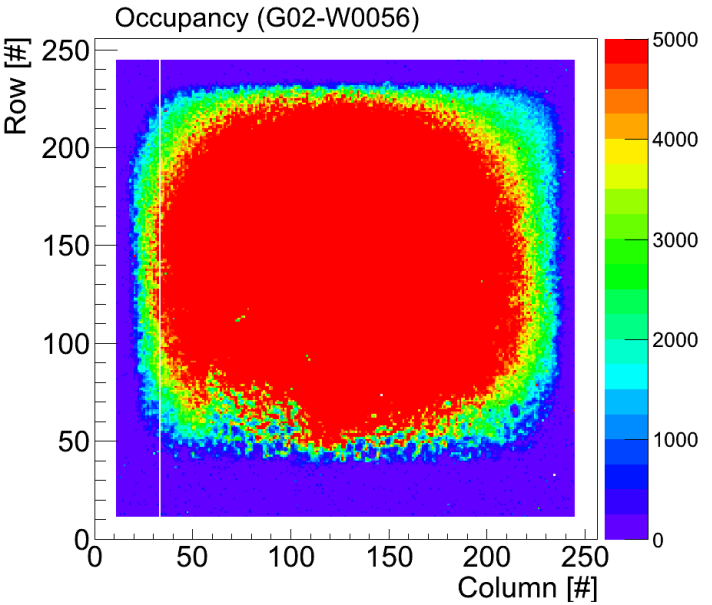


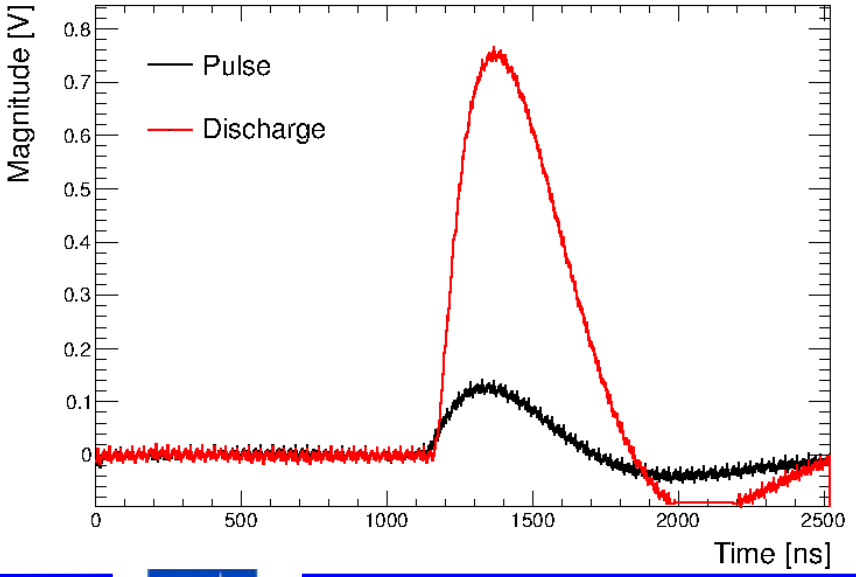


Some results



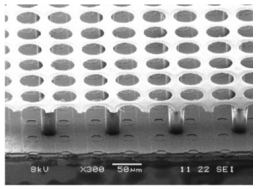




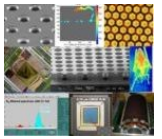


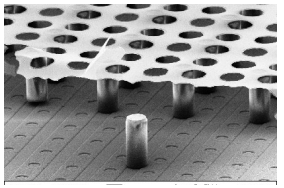
InGrids of batch 3 and 4 show good properties:

- In Ar:iButane (95:5)
  → more than 400 V
- Very small insensitive areas
- Chips survive thousands of discharges



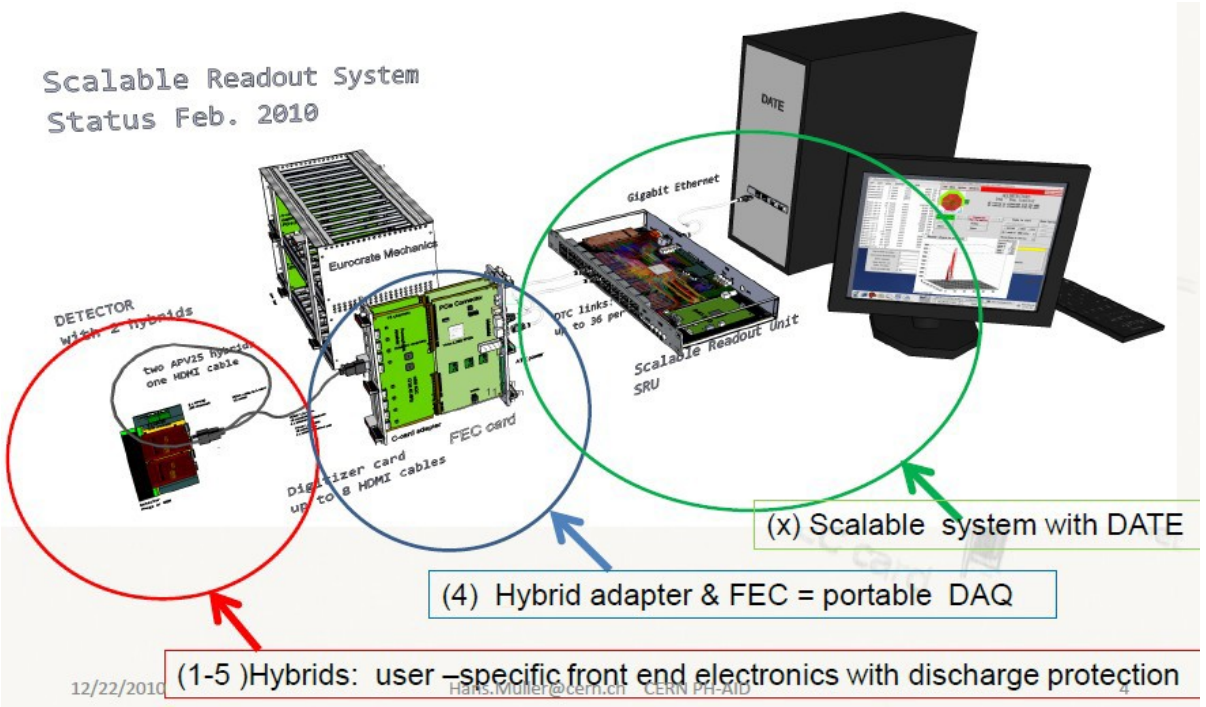
Timepix readout with SRS



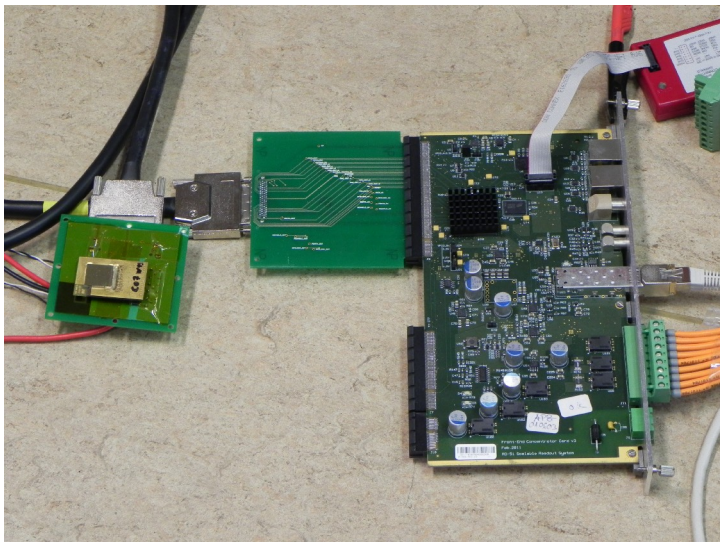


The Scalable Readout System is designed by the RD51 collaboration with CERN as a main developer. → See presentation of H. Muller

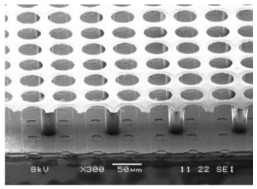
Idea: produce a flexible readout electronics, which can handle different chips (new FPGA code, chip carrier), which many groups can use



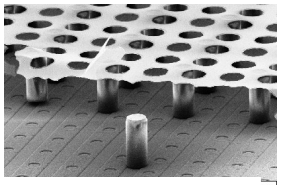
U. Bonn is developing a readout for the Timepix chip.

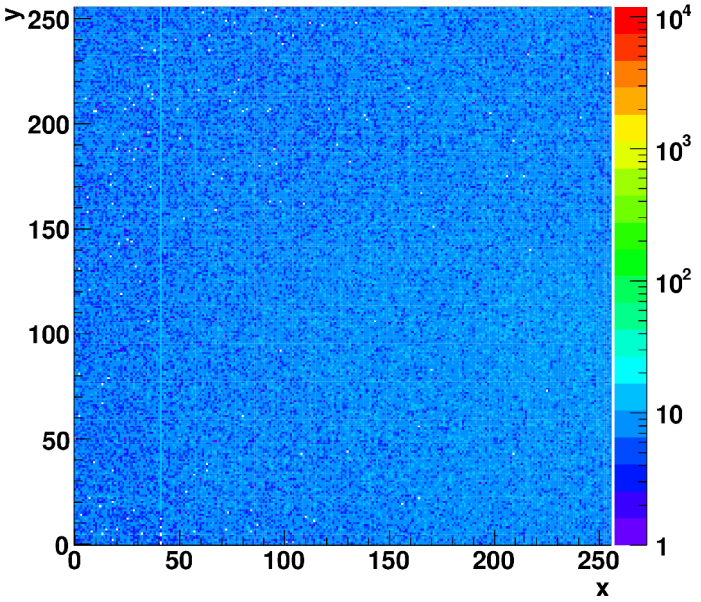


Operation has been demonstrated for a eight chip, more functionality has to be added.

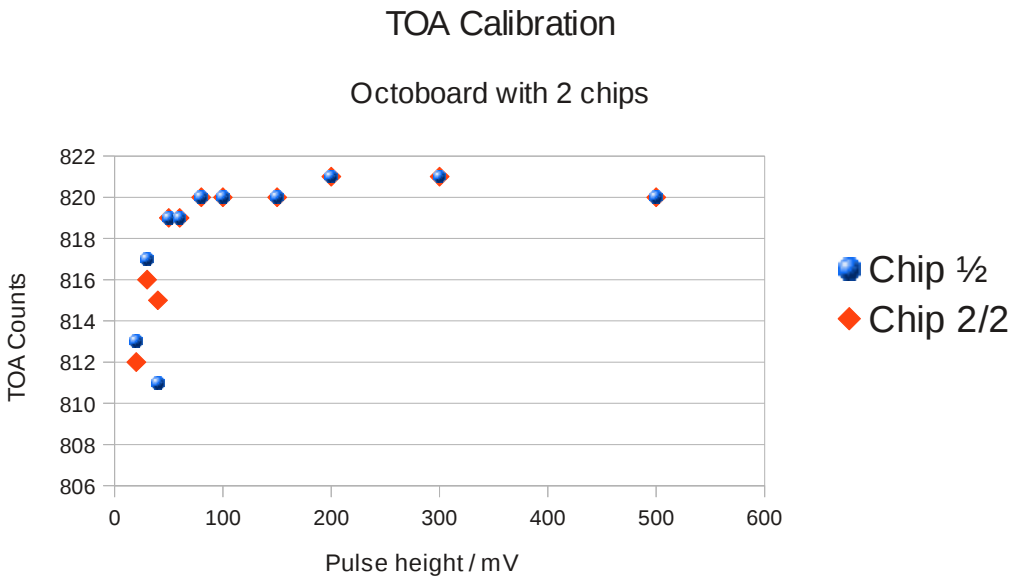


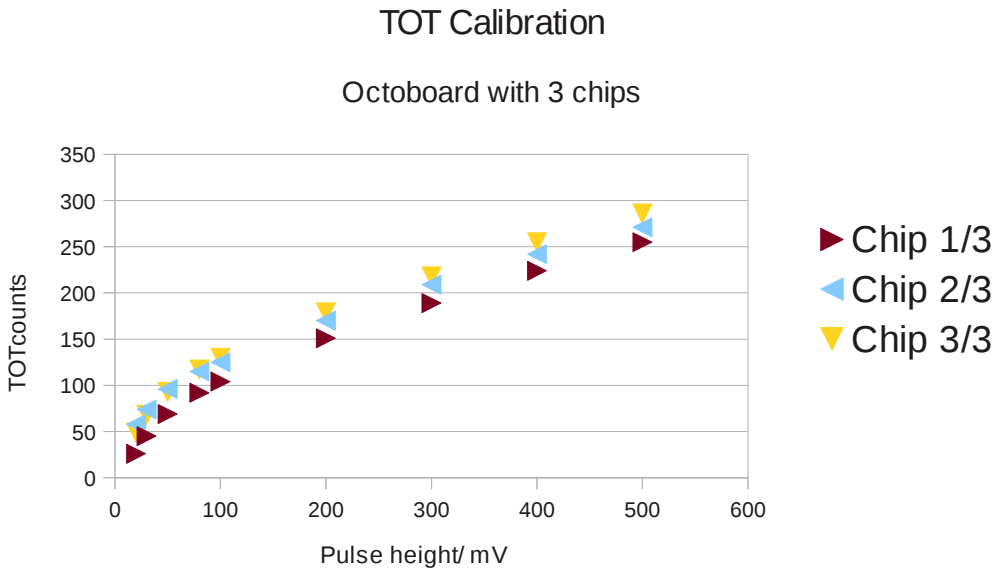
Calibration Results (I)

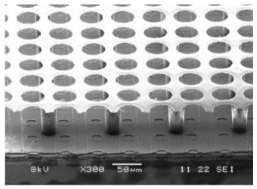




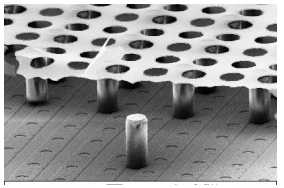
Distribution of threshold equalization bits of chip 3 on octoboard

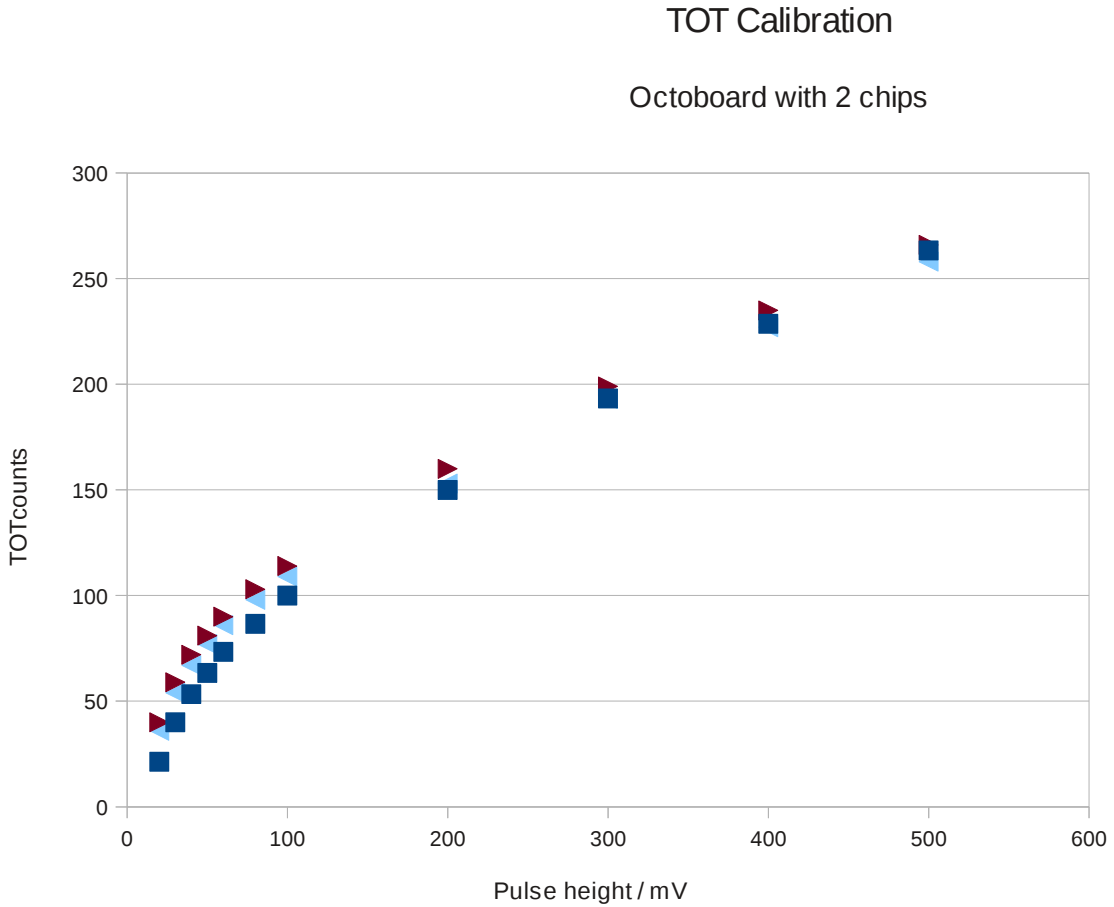


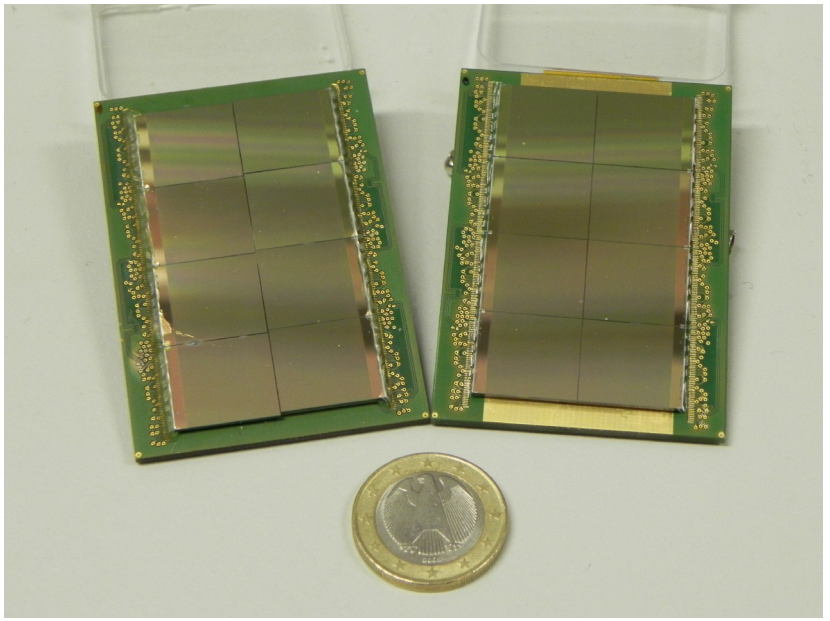




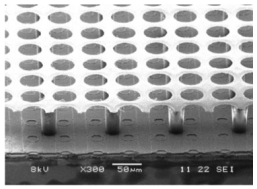
Calibration Results (II)



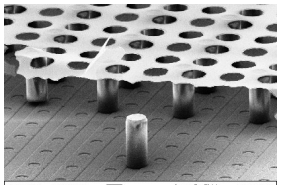


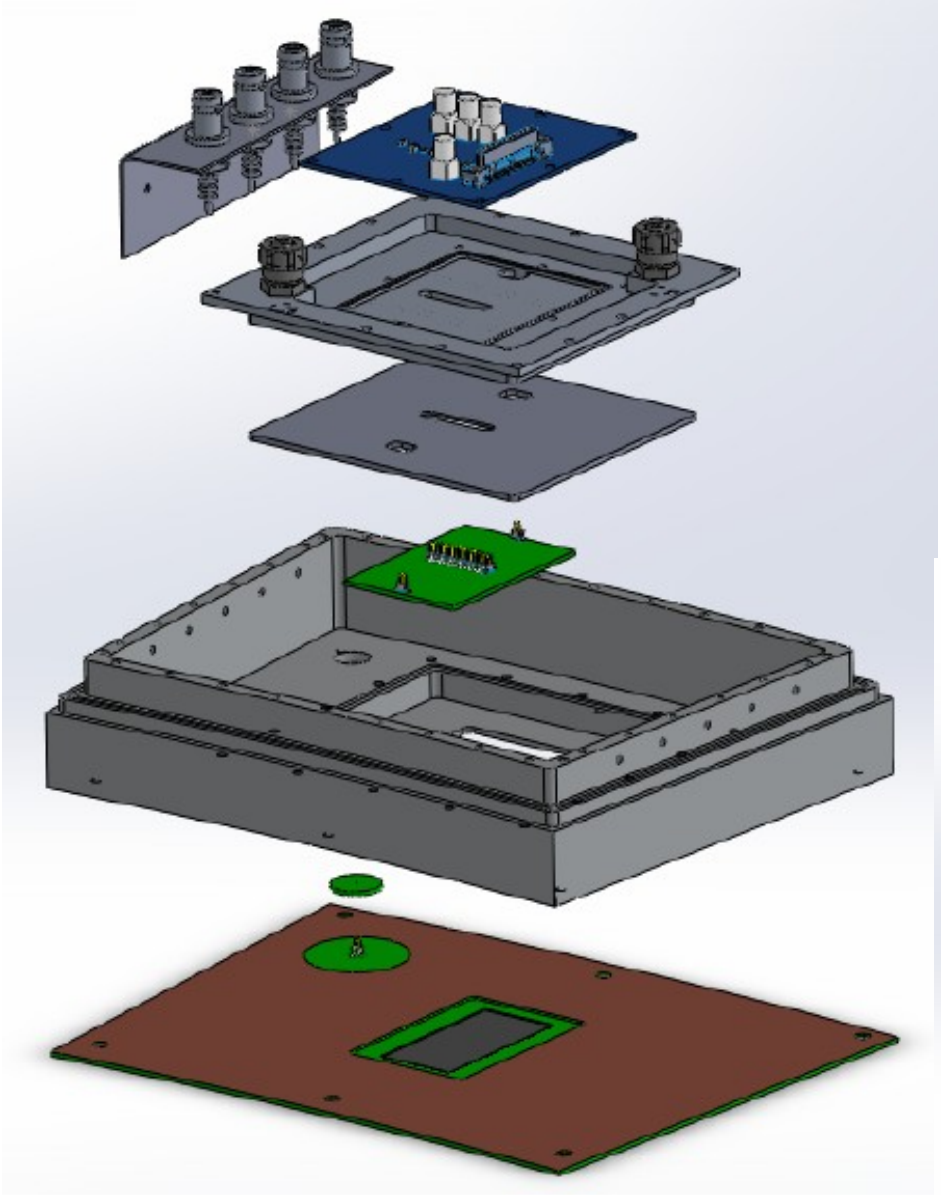


2 boards with bare Timepix chips have been completed – it works.
First board with InGrids has started.



Short Term Plan

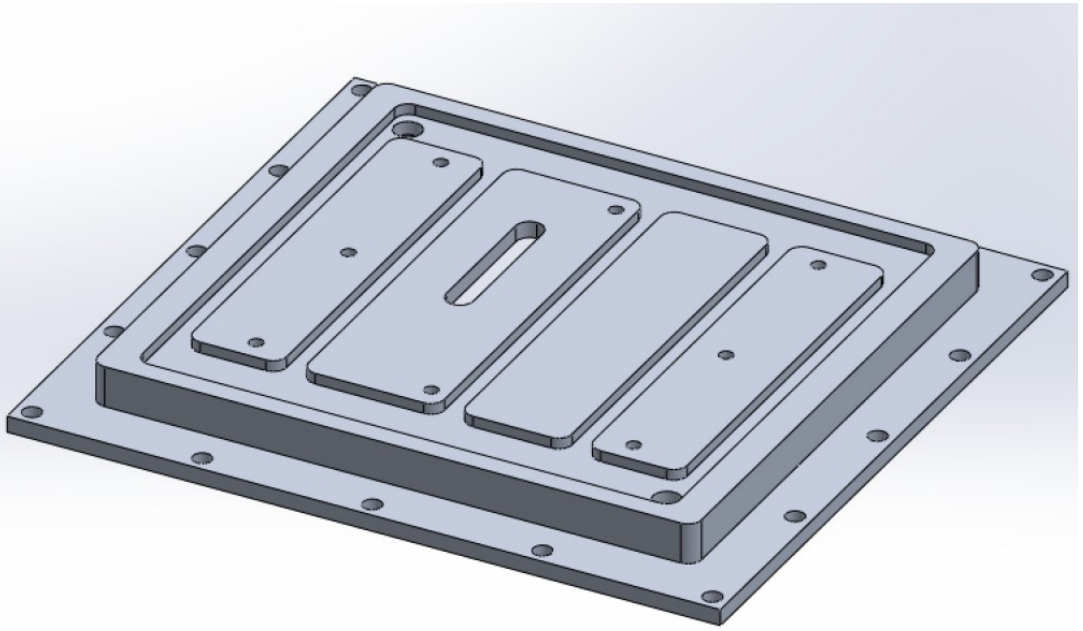


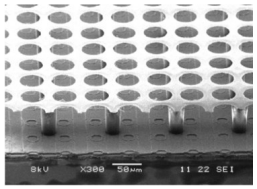


2 LCTPC modules shall be tested at the DESY test beam at the end of March with 8 Timepix chips:

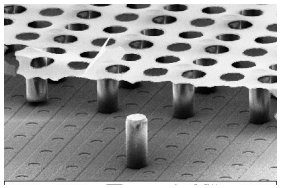
- Tripe GEM with bare Timepix chips
- 8 InGrids

Cooling will be done with water.

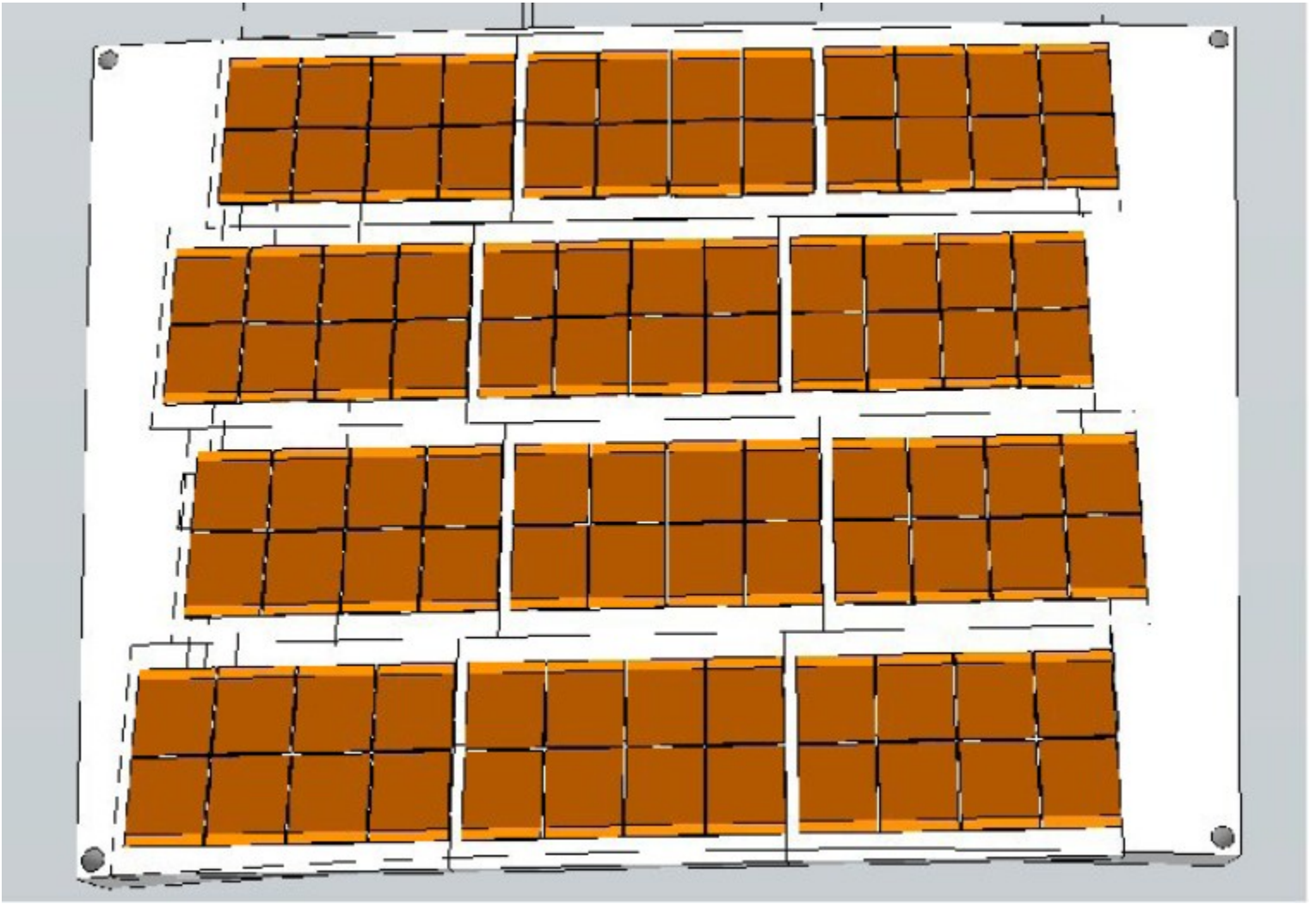


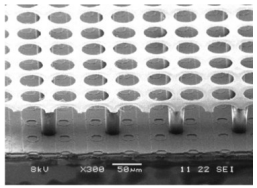


Mid-Term Plan

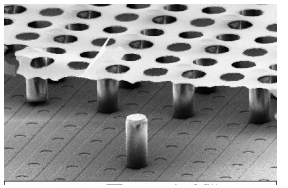


Module completely covered with Timepix chips (~100-120).





Summary and Outlook



InGrids have shown excellent performance:

- Energy resolution of $\sigma_E/E \sim 5\ \%$ (at 5.9 keV)
- Spatial resolution only limited by diffusion.
- High efficiency for single electron detection.

Production techniques are well advanced, the reliability of the production process has to be optimized.

Several readout systems optimized for large number of chips has been developed.

Large systems (~100 chips) will be operated soon.

Further R&D on InGrids are planned (resistive grid, all ceramic,...)

New Timepix-3 could be available this year.

Acknowledgment: This presentation shows the work of many people at NIKHEF, U. Twente/MESA+, U. Bonn, IZM, CEA Saclay.