# Towards large scale pixelated gaseous detectors

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On behalf of the LCTPC collaboration

Outline:

- Pixelated gaseous detectors: Motivation & History
- Timepix and InGrid
- Detector setup and readout
- 2013 testbeam at DESY

GEFÖRDERT VOM

Bundesministerium für Bildung und Forschung

MPGD2013, July 3, Zaragoza

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Photoelectron "tracks", distinction between photons, MIPS, alphas

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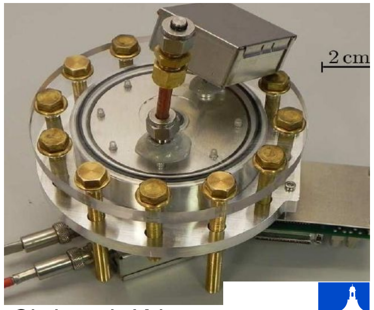
Photoelectron “tracks”, distinction between photons, MIPS, alphas

<u>Possible applications:</u>

- Rare event searches: CAST, DARWIN
- Tracking: GOSSIP, ILC

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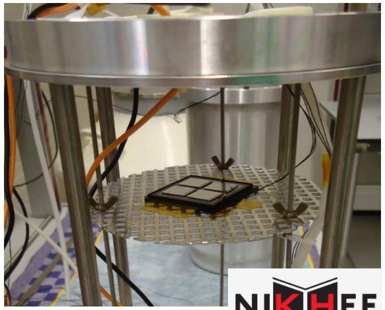

Rolf Schön NIKHEF

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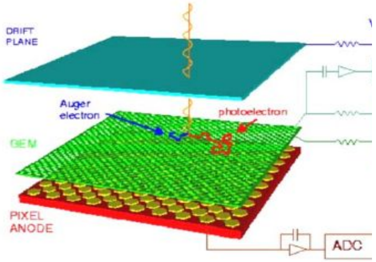

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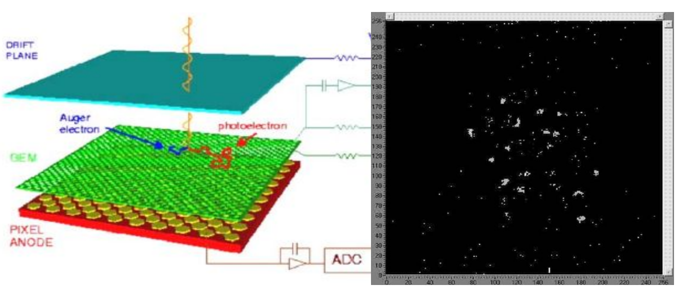

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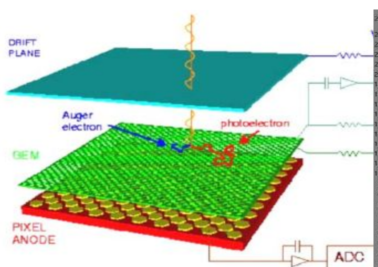


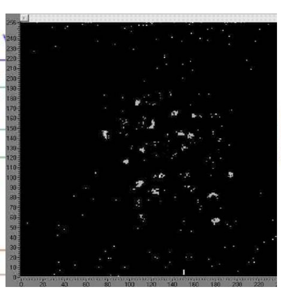

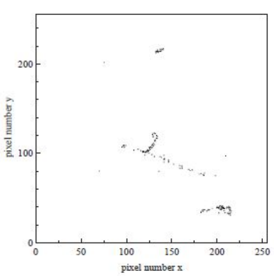

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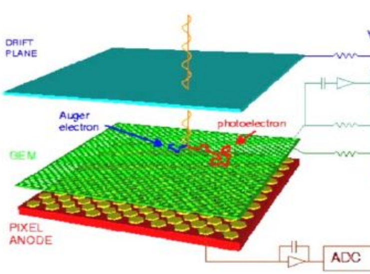

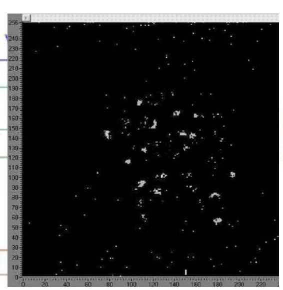
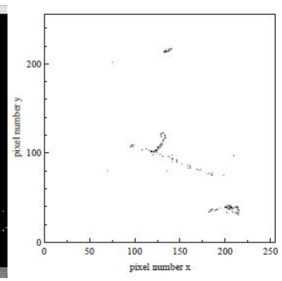

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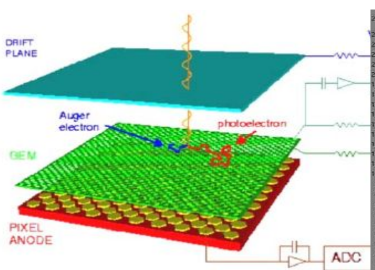


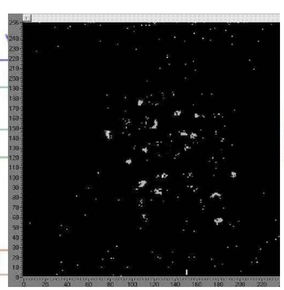

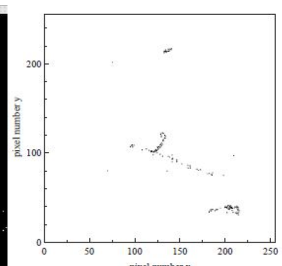


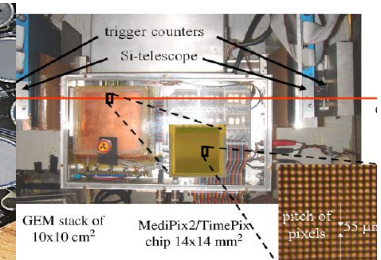

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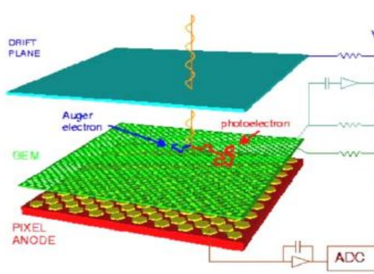
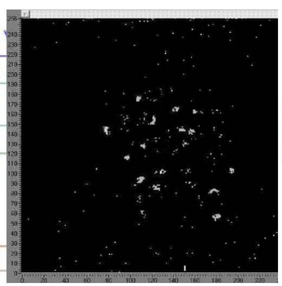
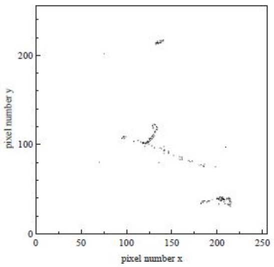
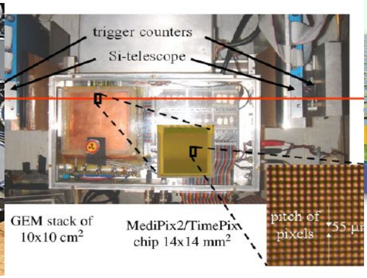
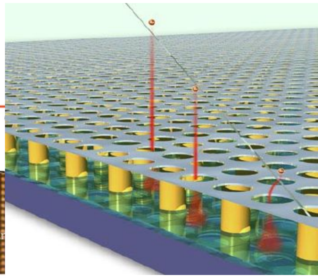
- 2009: Performance and prospects of GridPix and Gossip detectors
  H. van der Graaf, F. Hartjes, A. Romaniouk, ATLAS note ATL-P-MN-0016



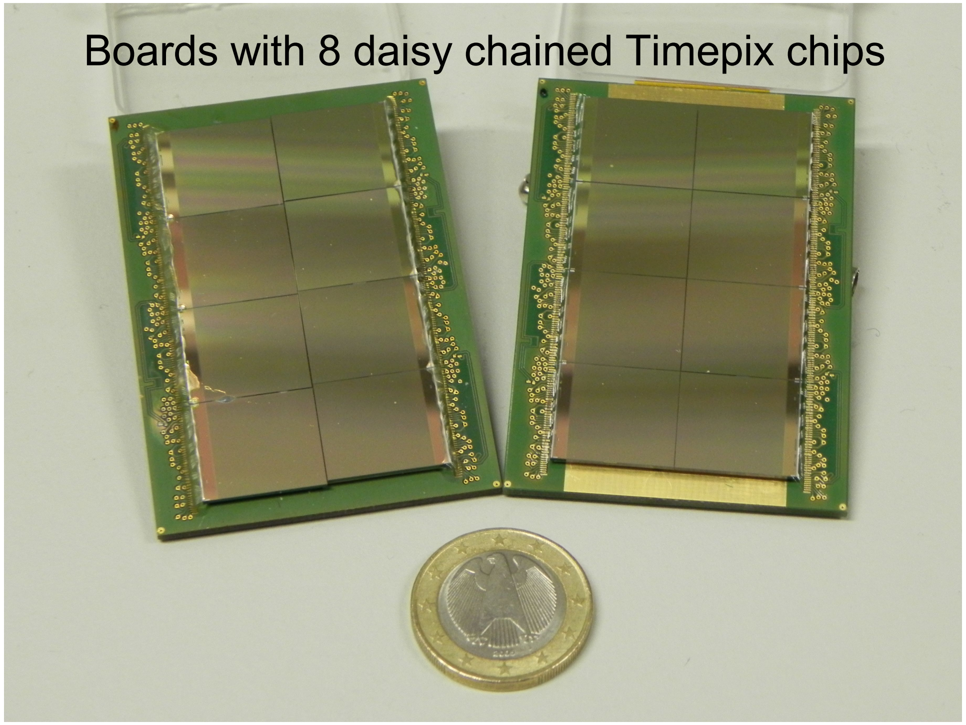





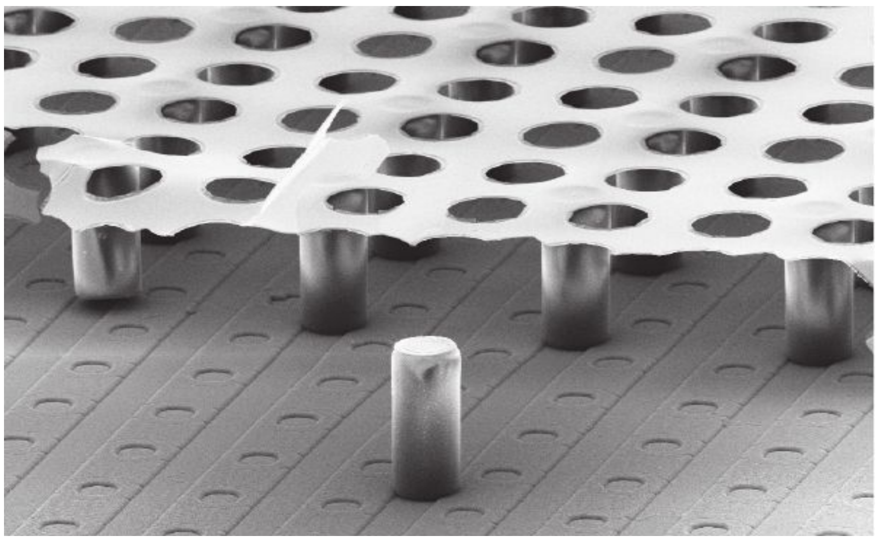
# Timepix chip

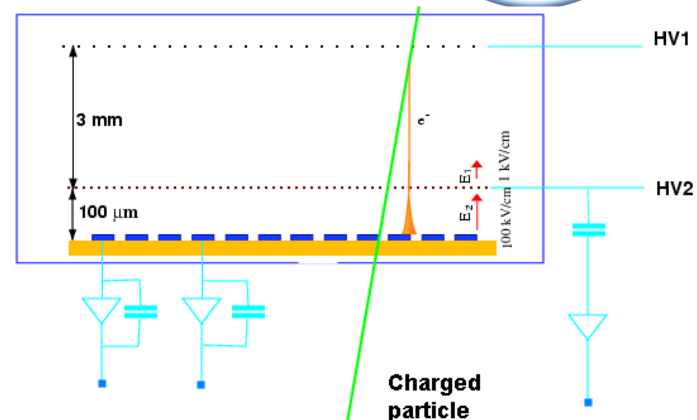
- Readout chip used for many applications
- Characteristics:
  - Active surface: 1.4 x 1.4 cm², 256 x 256 pixel array
  - Pixel size 55 x 55 µm²
  - 14 bit counter in each pixel (measure arrival time or charge)
  - Analog part: single threshold typical at ~500$e^-$ (ENC ≈ 90$e^-$)

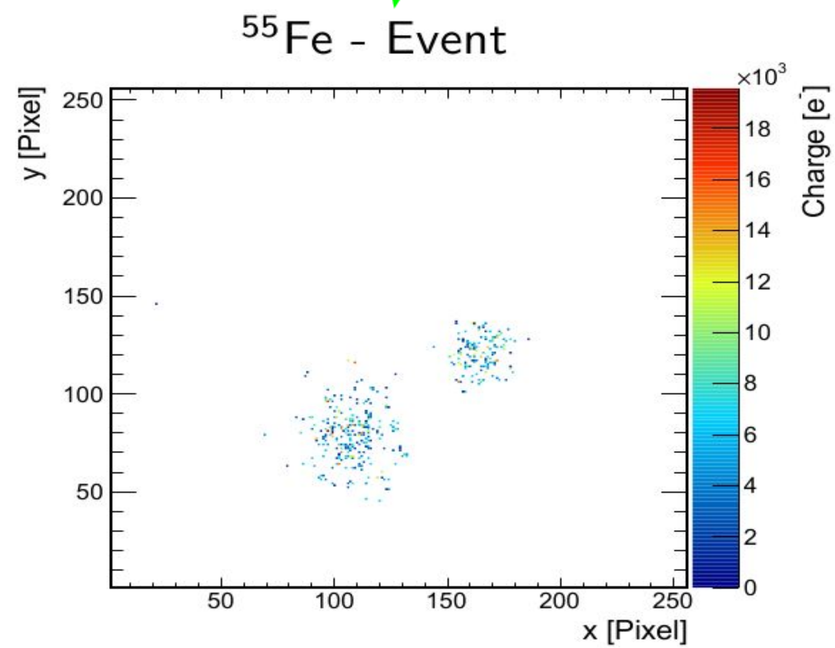


# Timepix+Micromegas=InGrid

- Aluminium mesh on chip
  - Hole to pixel alignment
  - Pillar height uniformity





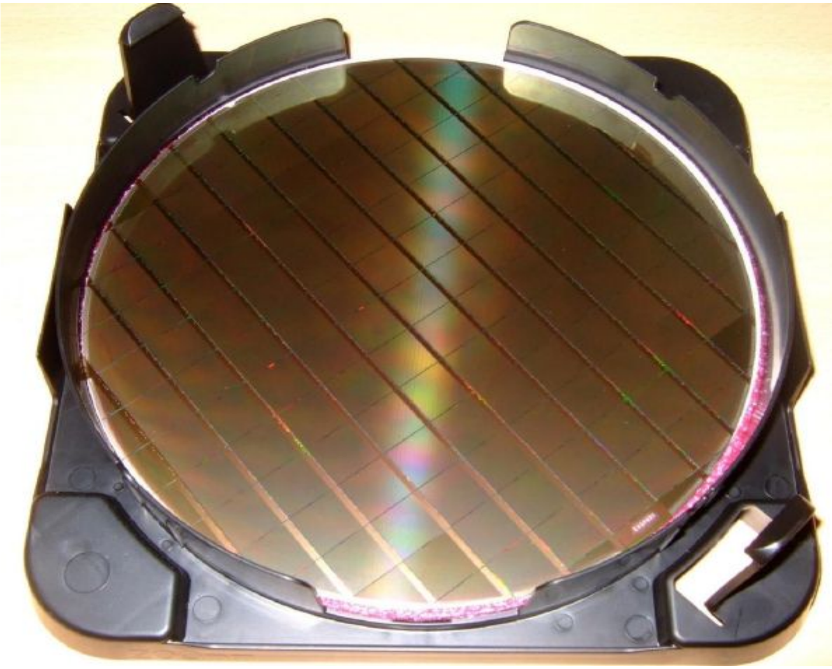




- Use photolithographic process
  - Pioneered and optimised by NIKHEF and University of Twente
  - Production on single chip basis

# Production on wafer scale

- High demand for InGrid chips:
  - R&D at Bonn, NIKHEF, Saclay
  - Equipment of larger surfaces

⇒ Production on wafer scale



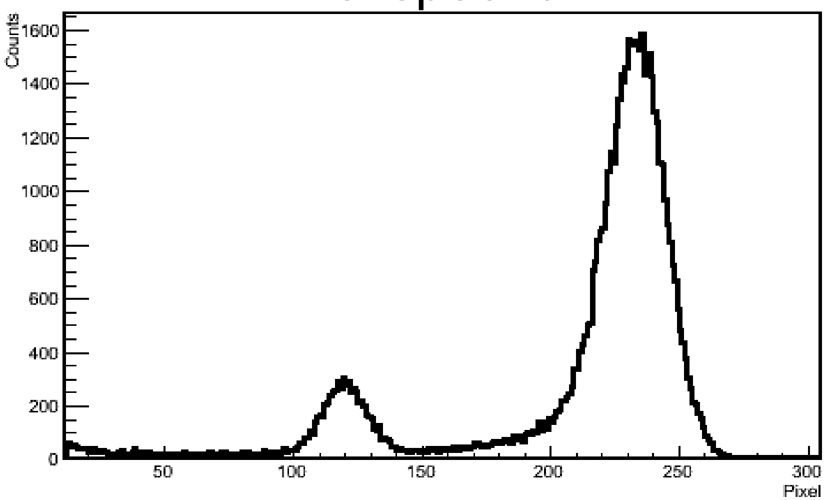
- 8 inch wafer = 107 chips

Fraunhofer IZM (Berlin)

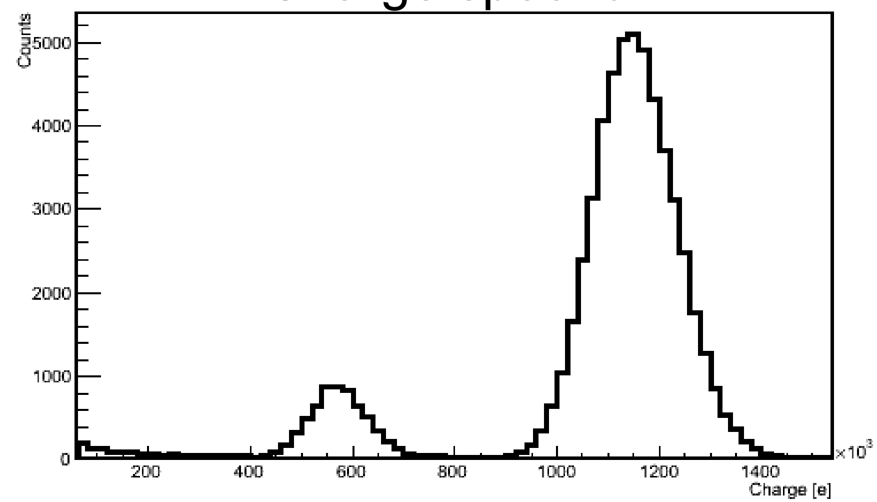
has machinery for post-processing

# InGrid testing

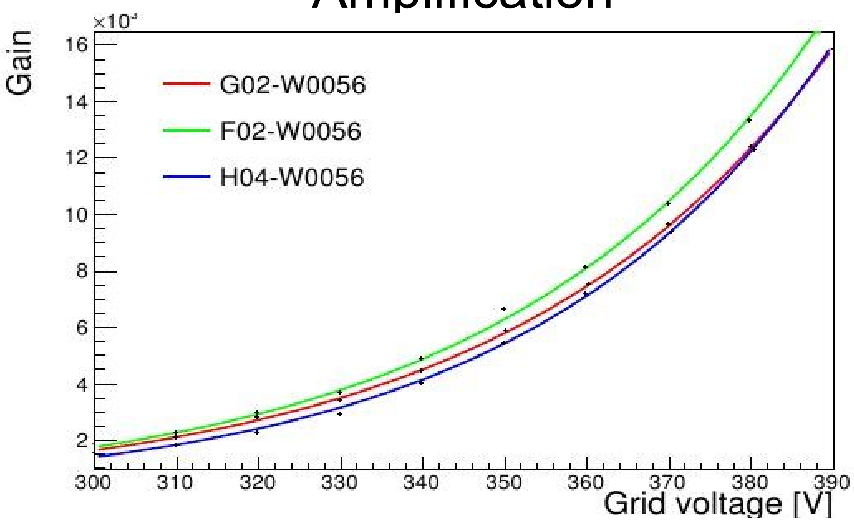
Pixel spectrum




Charge spectrum




Amplification




Performance in Ar/iButane (95/5)

- Energy resolution:

Pixel: $\frac{\sigma_N}{N} = 5.0\%$

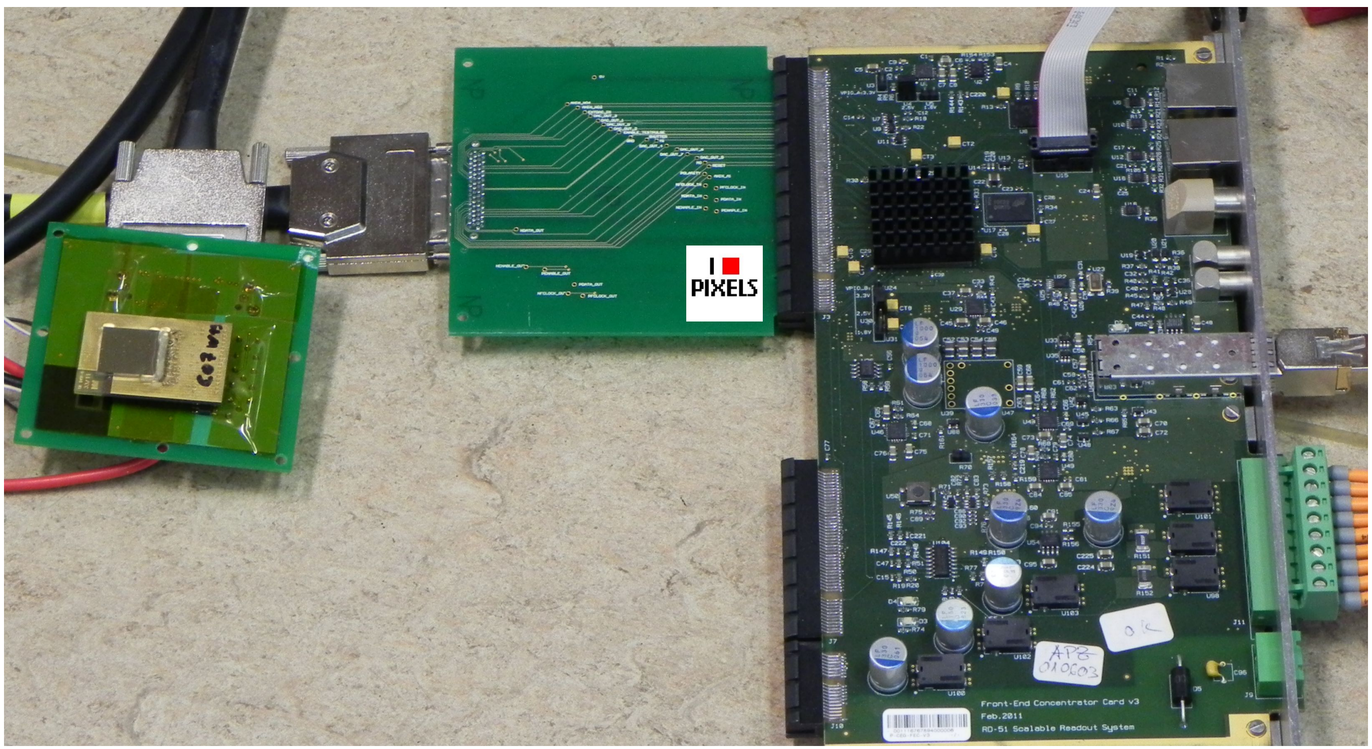
Charge: $\frac{\sigma_N}{N} = 6.7\%$

- Similar Gain for various devices

⇒ Performance similar to single chip production

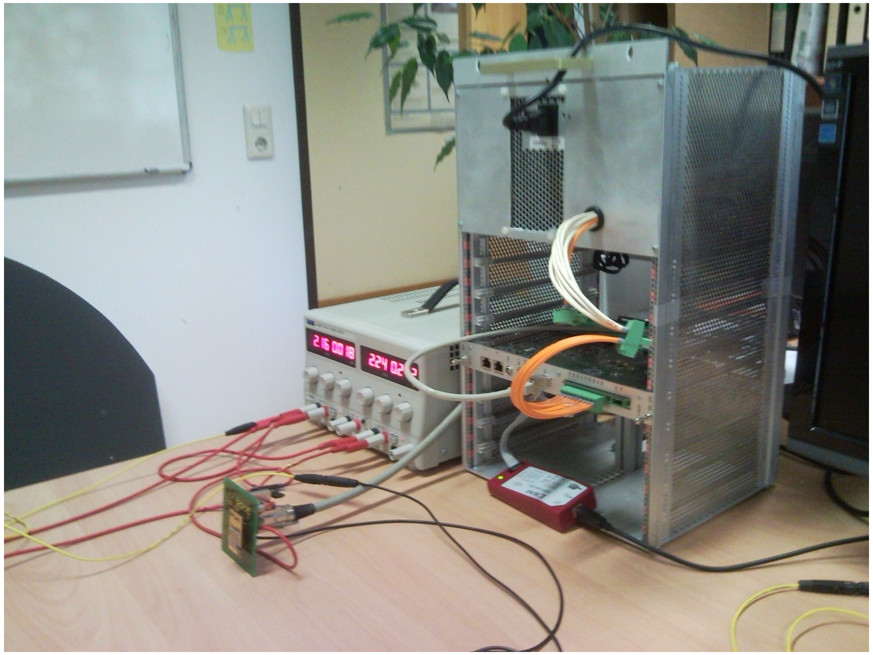
# Readout System

| Requirements: | & Solutions: |
| --- | --- |
| • Modular system | → Scalable Readout System (SRS) |
| • Availability of hardware | → Design adapter and chip carrier boards |
| • Open source code | → Develop FPGA code and DAQ software |
| • Readout maximum speed | → Zero suppression, multi-threading |



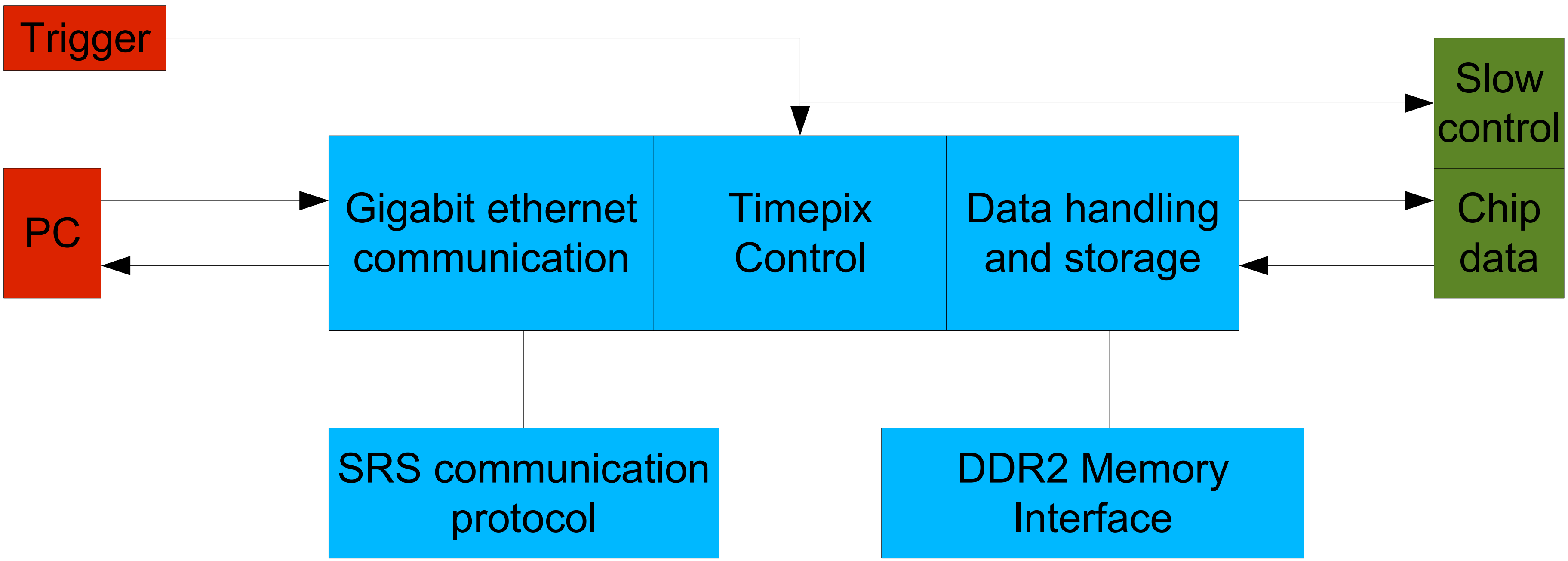
# Status Timepix+SRS Readout

- Functionality for data taking is implemented
  - Reset, set/read matrix and DACs (FSR),
  - Start/stop measurement, external trigger
  - DAC scan
  - Threshold equalisation
  - External test pulses



- Read out 8 chips in daisy chain (Octoboard)
- Next step: 4 Octoboards/FEC
- Small systems available for Xilinx board ML506/ML605

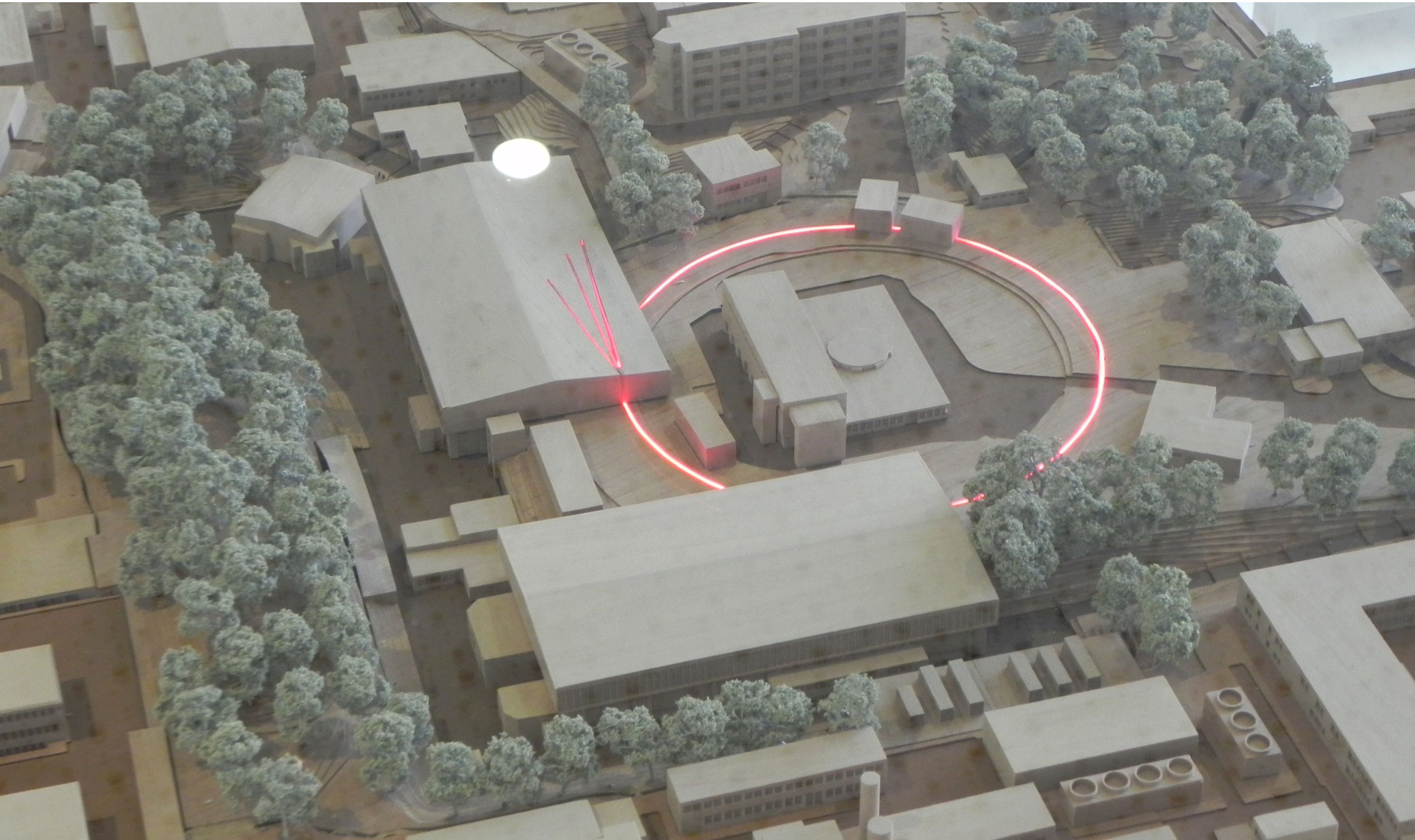
# FPGA Firmware




Some features:

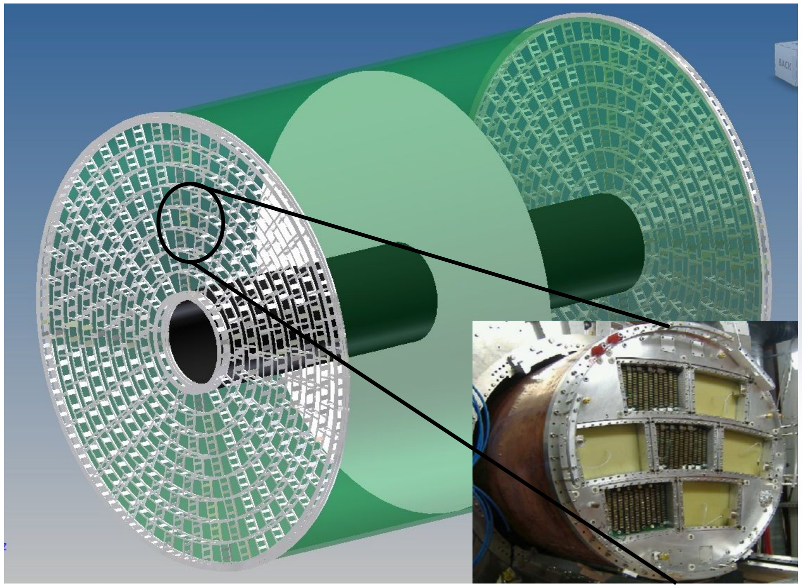
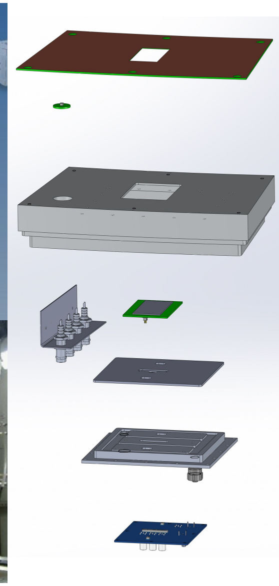
- Multi-threading (read chip while sending data of last frame)
- Zero suppressed data to PC
  ⇒ readout rate at theoretical maximum
- $I^2C$ for slow control coming soon

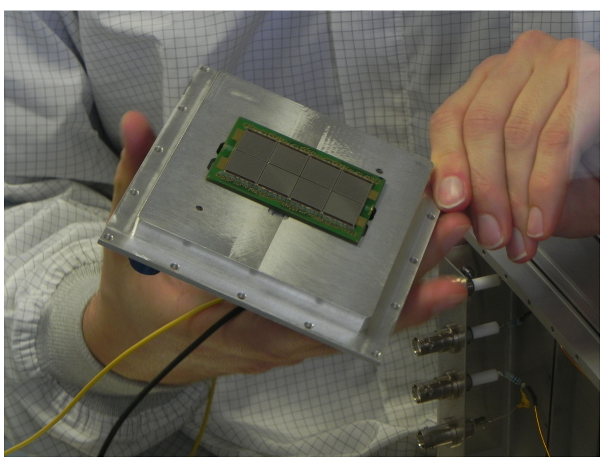
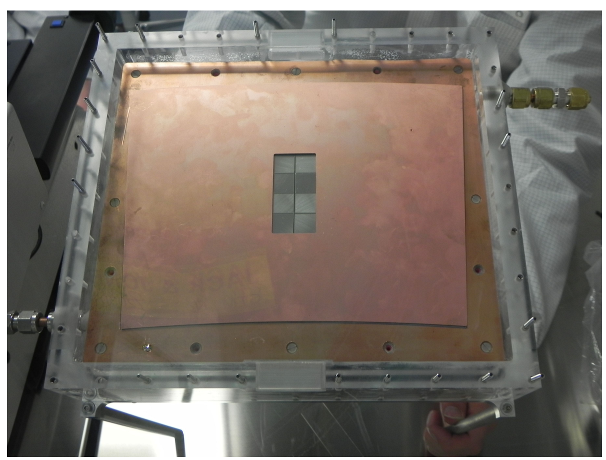
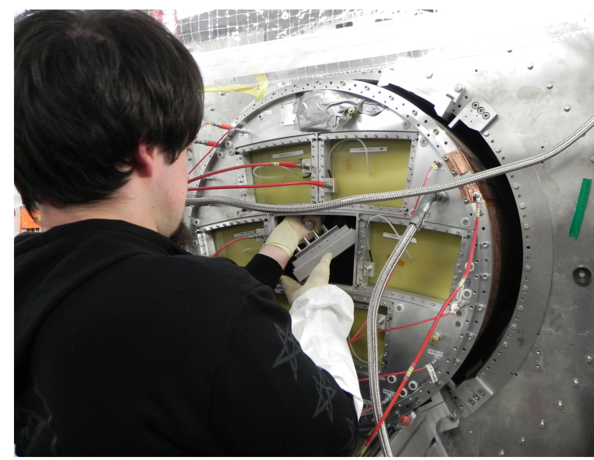
# SRS + Timepix @ test beam



# LCTPC Prototype

- Setup at DESY

# DESY Test beam

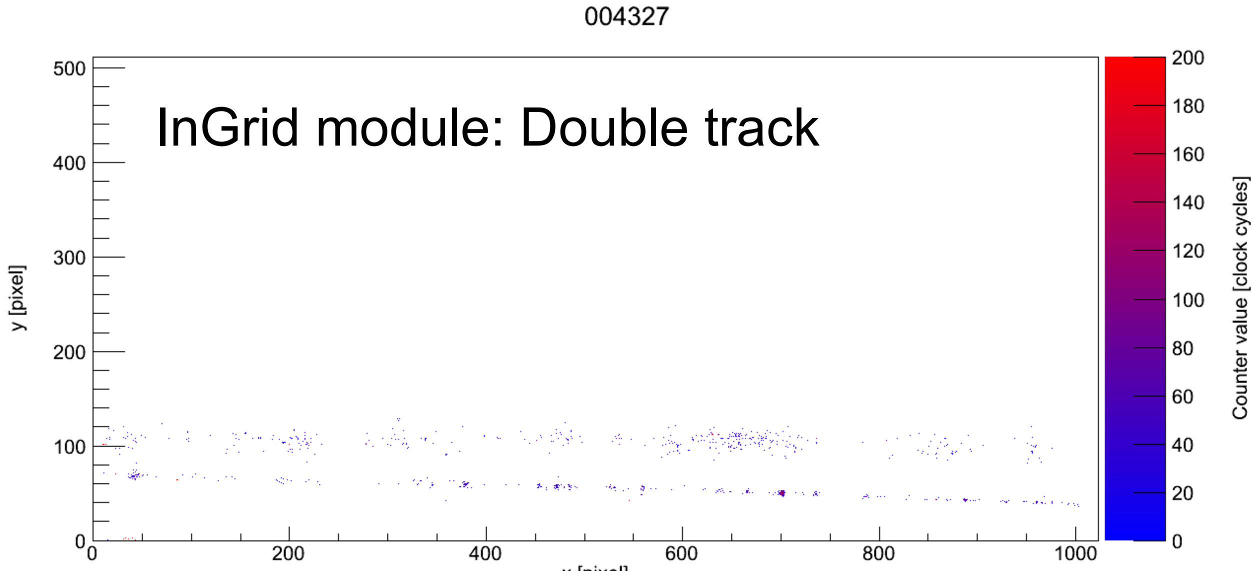
March/April 2013: 2 LCTPC octoboard modules

- Different amplification structures: GEM / InGrid
- Test of readout system

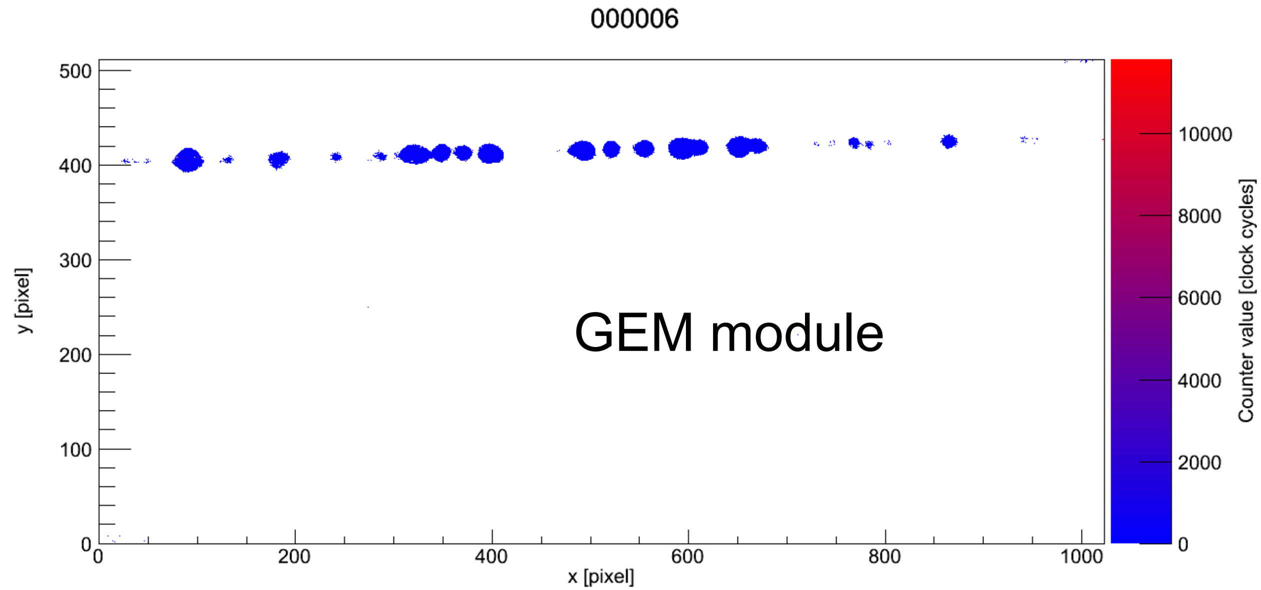
- Readout rate: 2,5 Hz; 40MHz clock
- Electron beam of up up 6 GeV
- ~ 2 Mio. frames recorded in T2K gas, including B = 1 T
- Testbeam program:
  - Voltage scan (gas gain, minimise field distortions)
  - z-scan, p-scan
  - Different angles

- Data analysis (in MARLIN TPC) by Andrii Chaus and Robert Menzen has just started.

# DESY Test beam




Online event displays



# Preliminary Analysis: Cuts

Dataset for first analysis:

z-scan, B=0 T, $E_{Drift}$ = 230 V/cm ($D_T$ = 311 μm/√cm)

⇒ tracks parallel to x-axis

Cuts:

- Only hits within shutter window
- More than 200 hits per track

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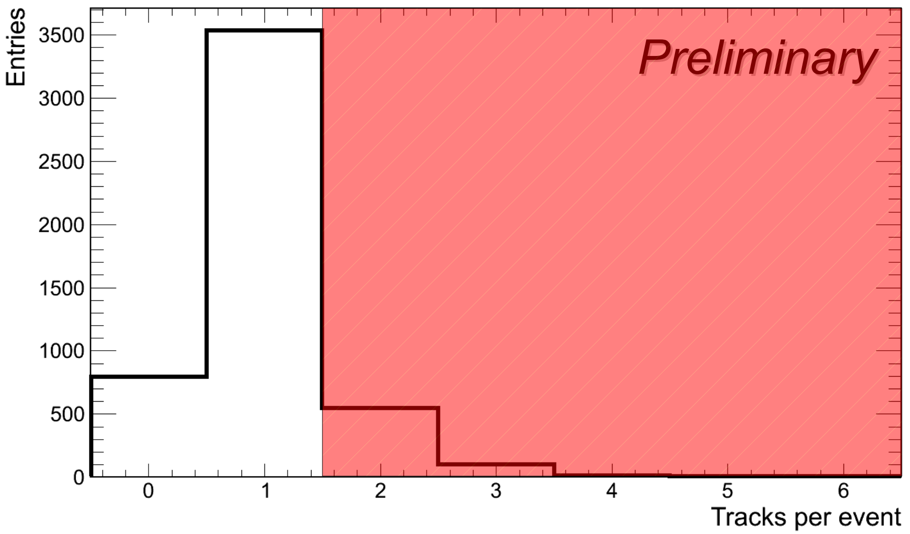
- Only single track events



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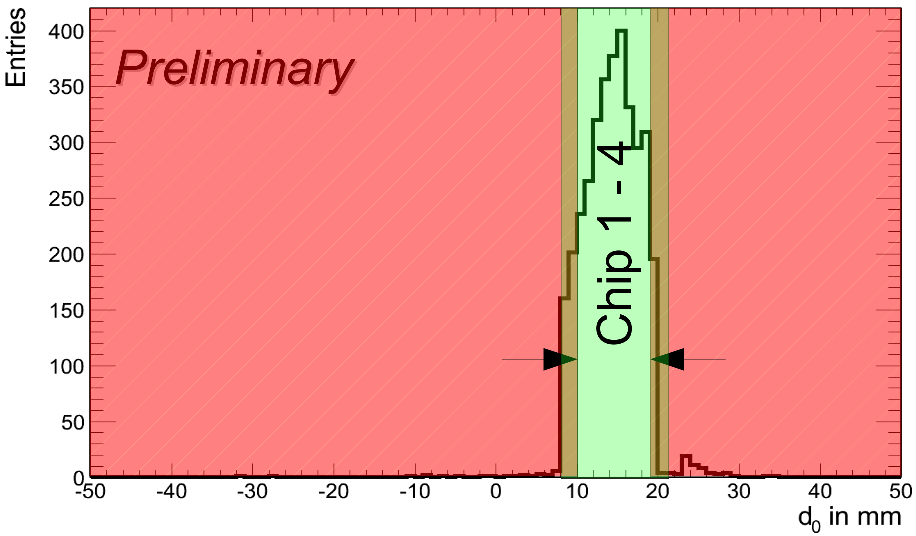
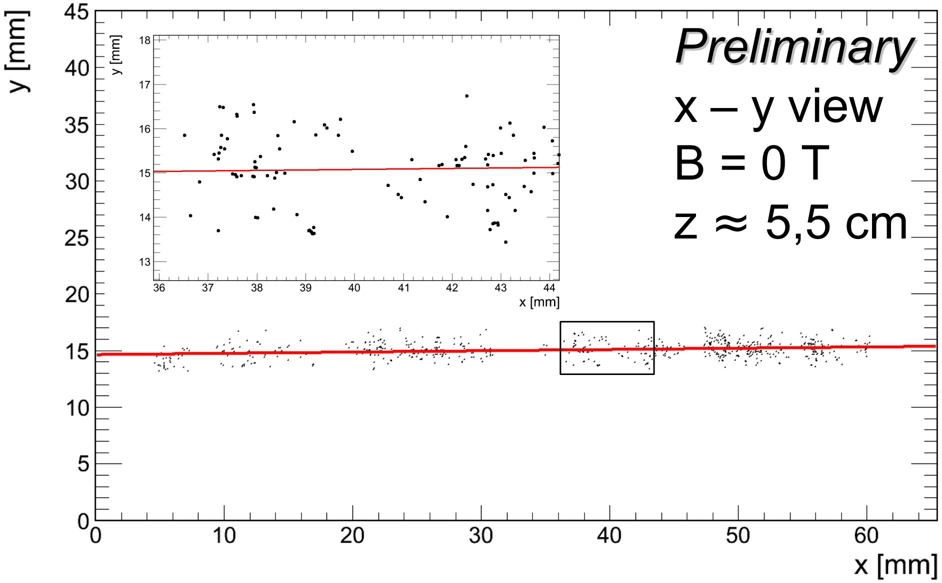
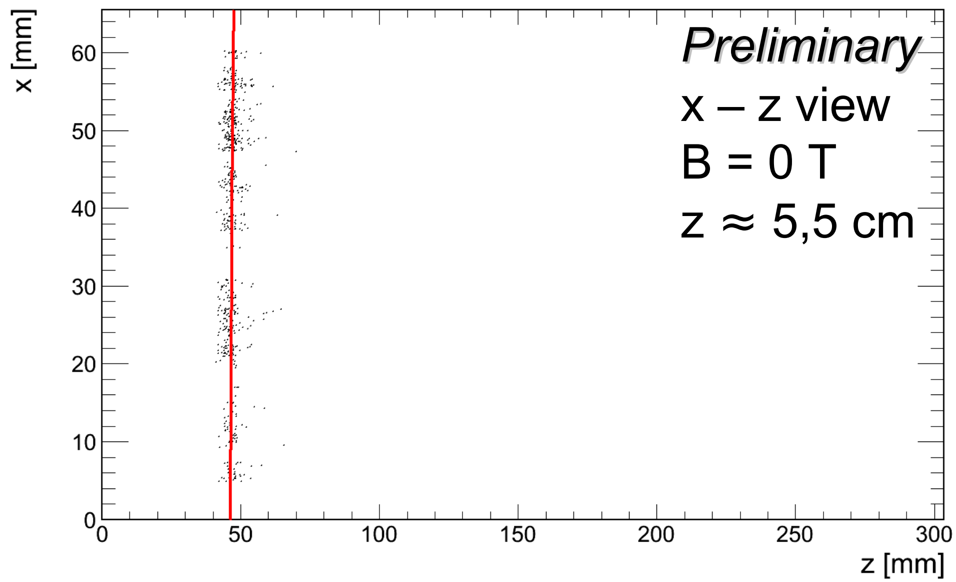


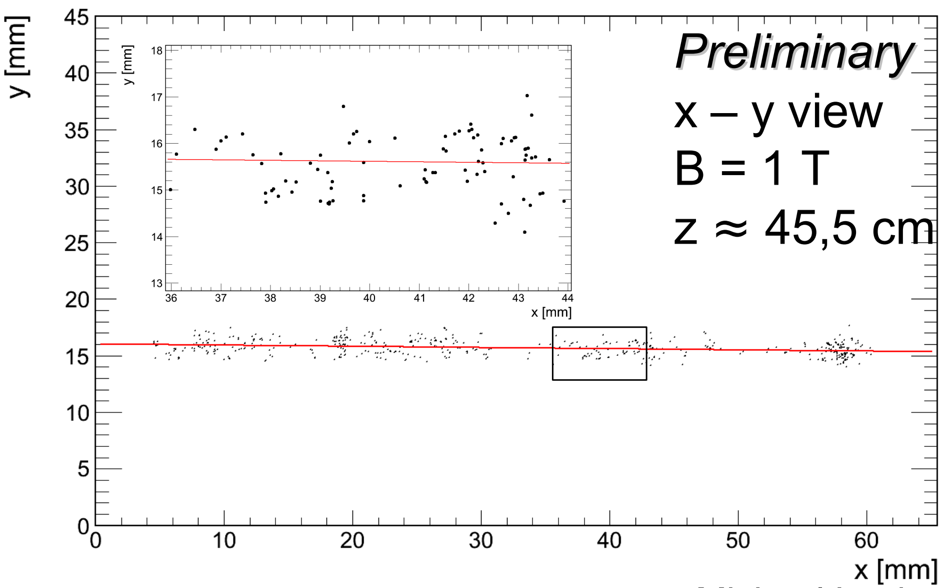

Cuts:

- Only hits within shutter window
- More than 200 hits per track
- Only single track events
- Tracks centred on lower chip row (z dependent)

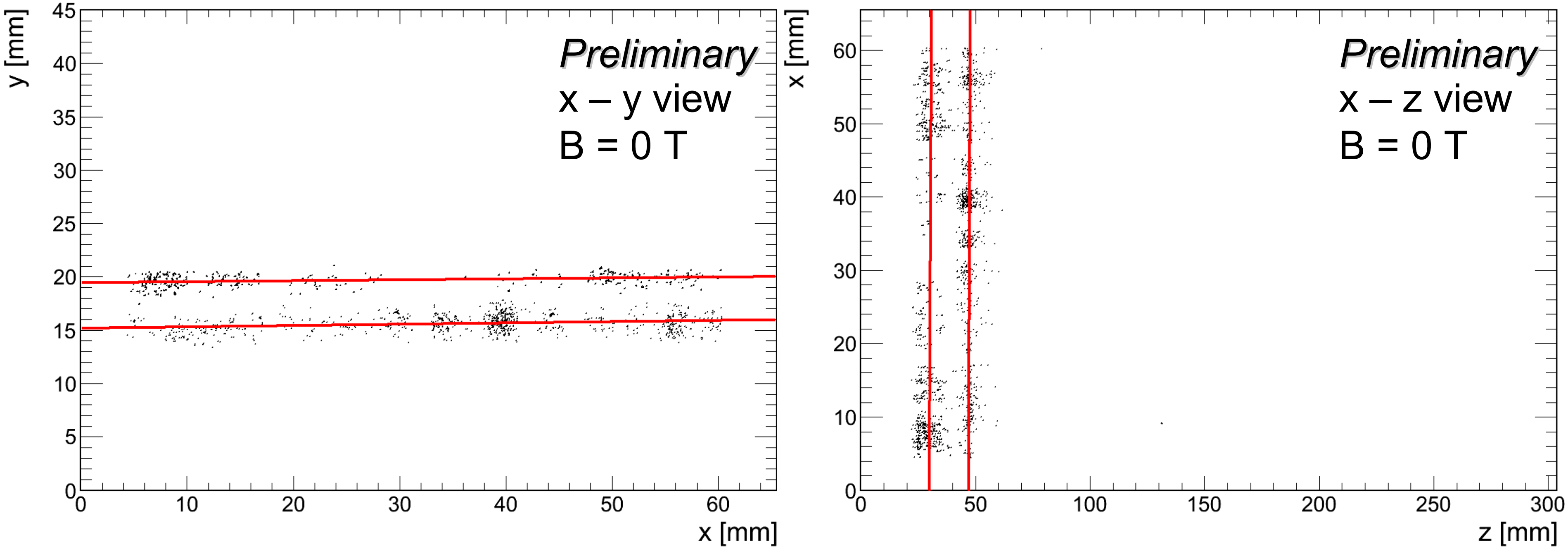
# Reconstructed tracks



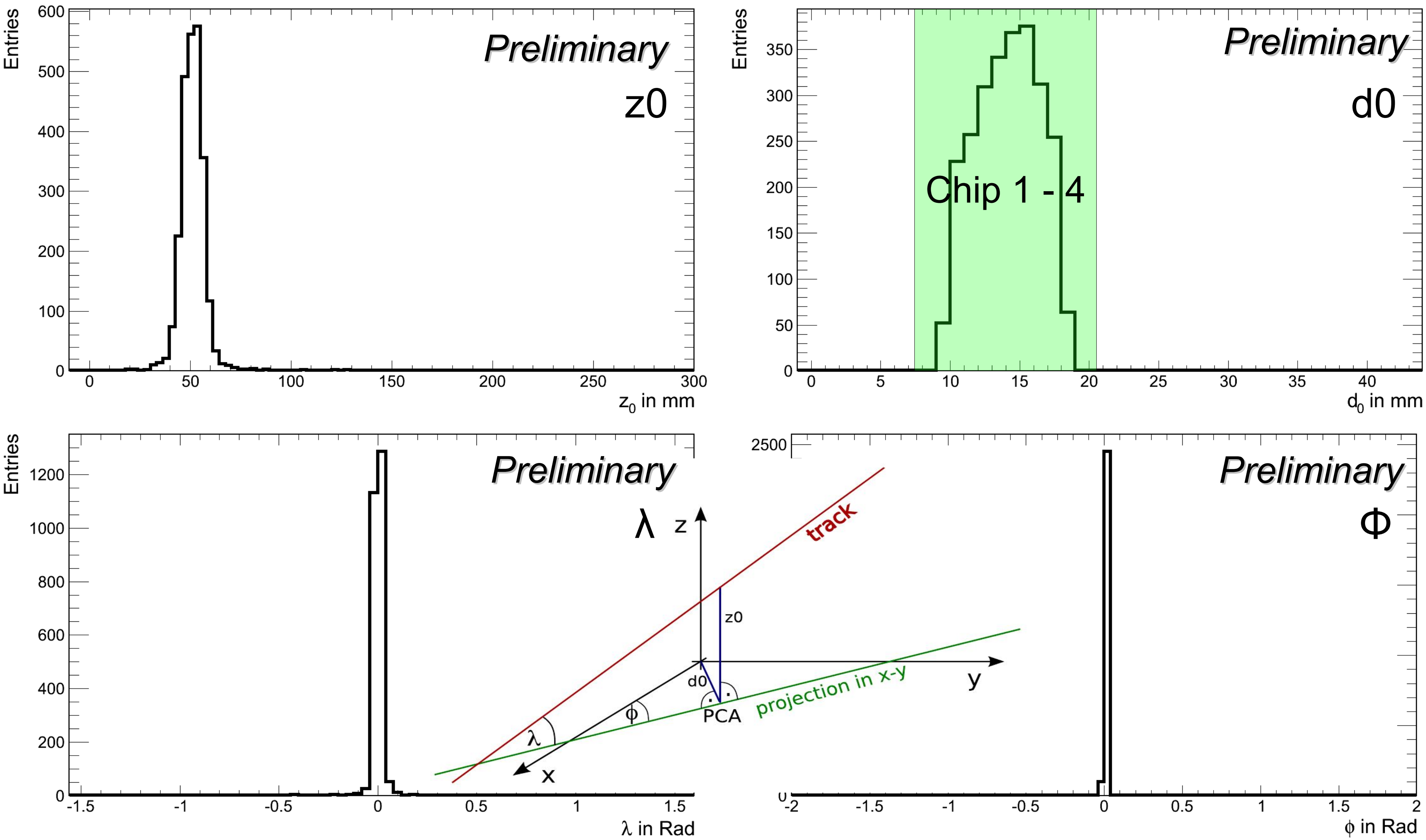



# Reconstructed double tracks



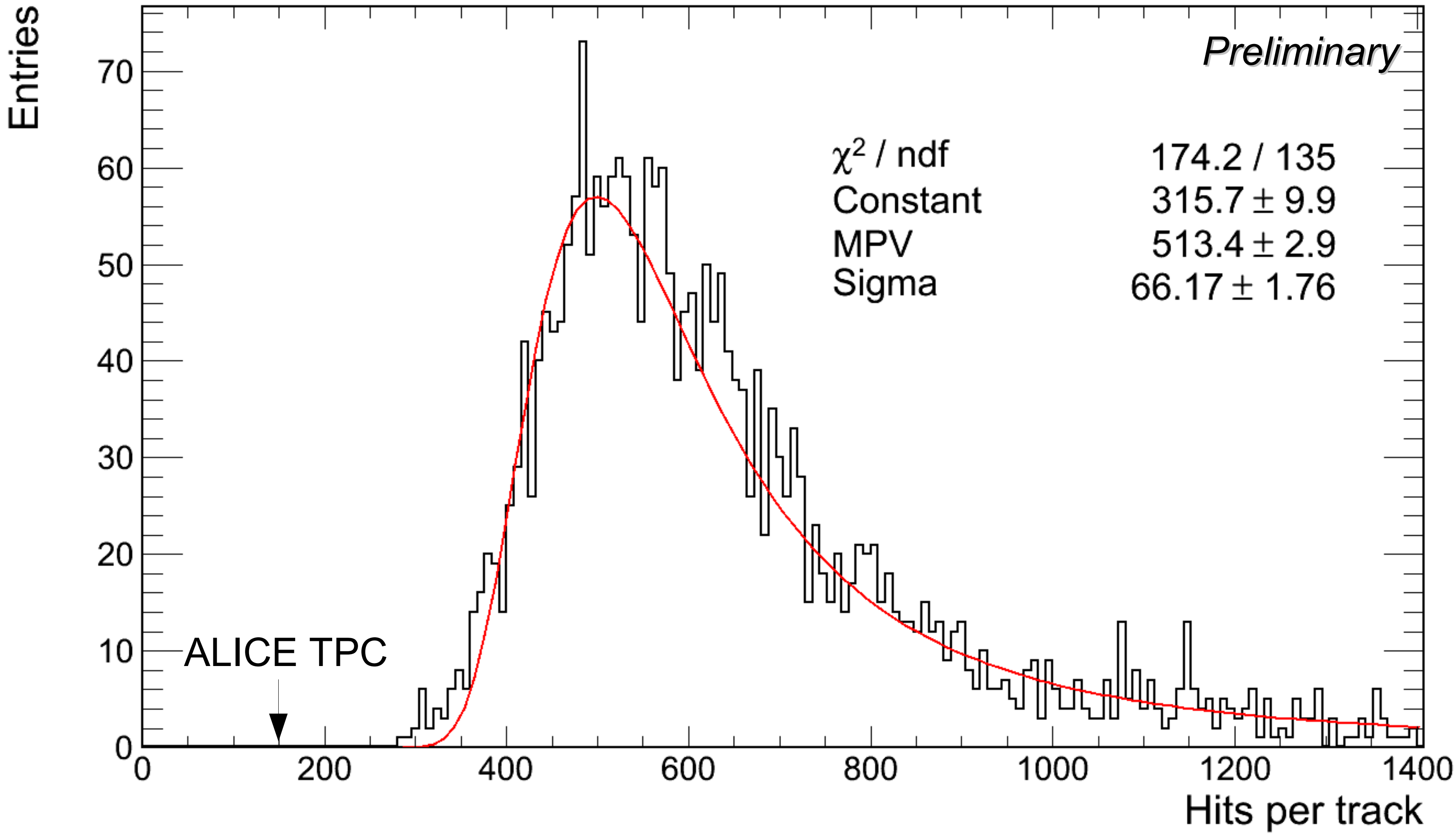
# Track parameters

Run: z = 5,58 cm, B = 0 T

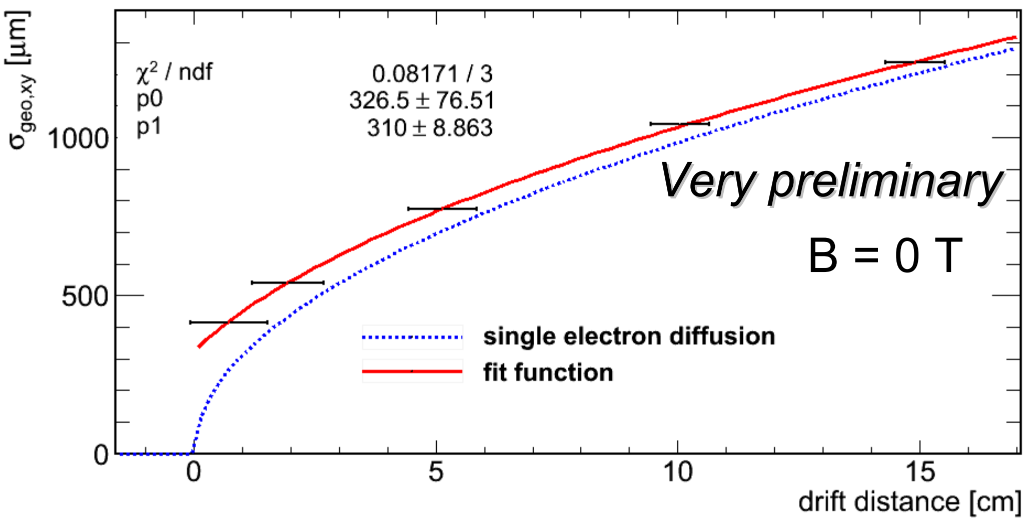


# Hits per tracks

B = 0 T, z = 5,58 cm, track length ≈ 5,6 cm



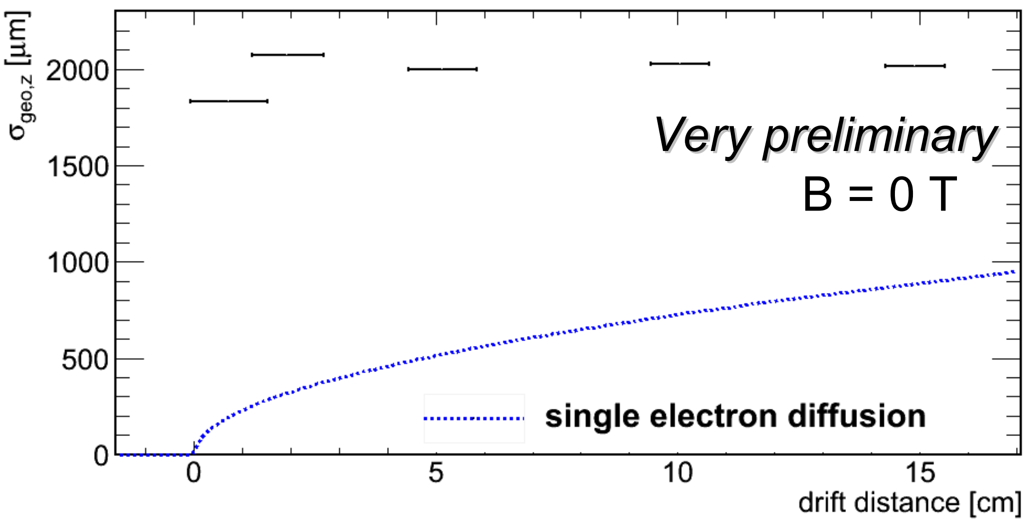
# Preliminary z-scan results




Fit function $f(x)=\sqrt{P0^2+P1^2 \cdot z}$

P0: intrinsic x-y resolution 327 µm dominated by field distortions

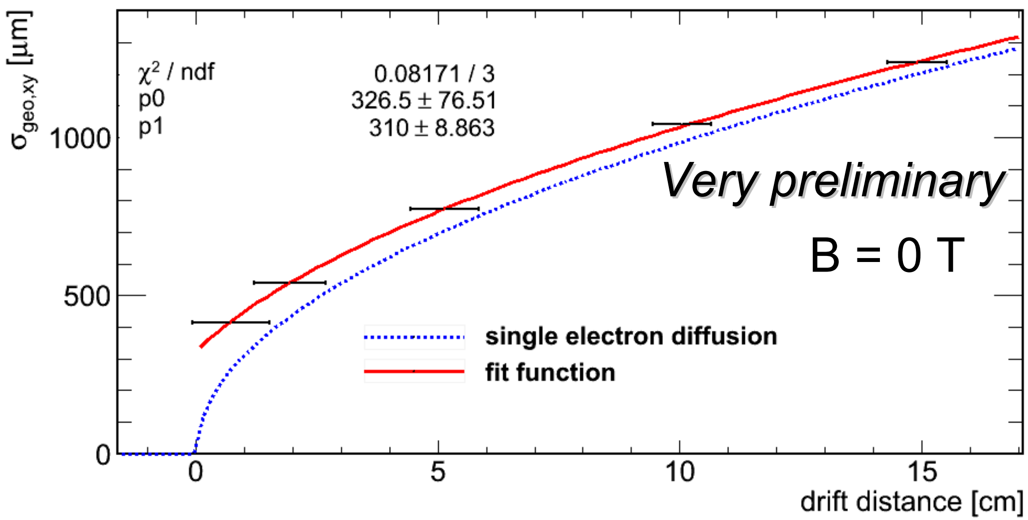
P1 = 310 µm/√cm: diffusion in T2K for E = 230 V




z resolution dominated by

- Clock frequency (25 ns time bins)
- Fast T2K gas ($v_{Drift}$ ≈ 73 mm / µs)
- Timewalk effect

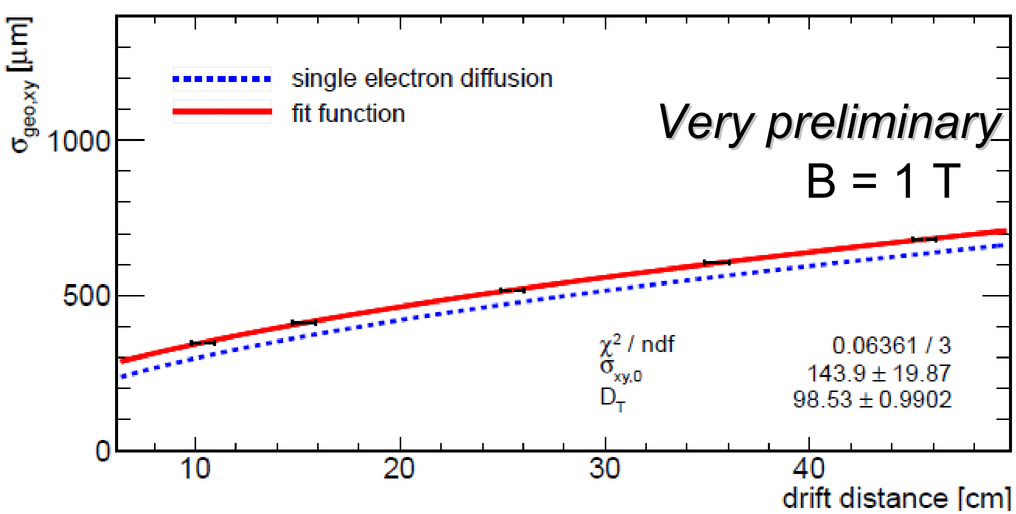
# Preliminary z-scan results




Fit function $f(x)=\sqrt{P0^2+P1^2\cdot z}$

P0: intrinsic x-y resolution 327 μm dominated by field distortions

P1 = 310 μm/√cm: diffusion in T2K for E = 230 V




B = 1 T

# Summary

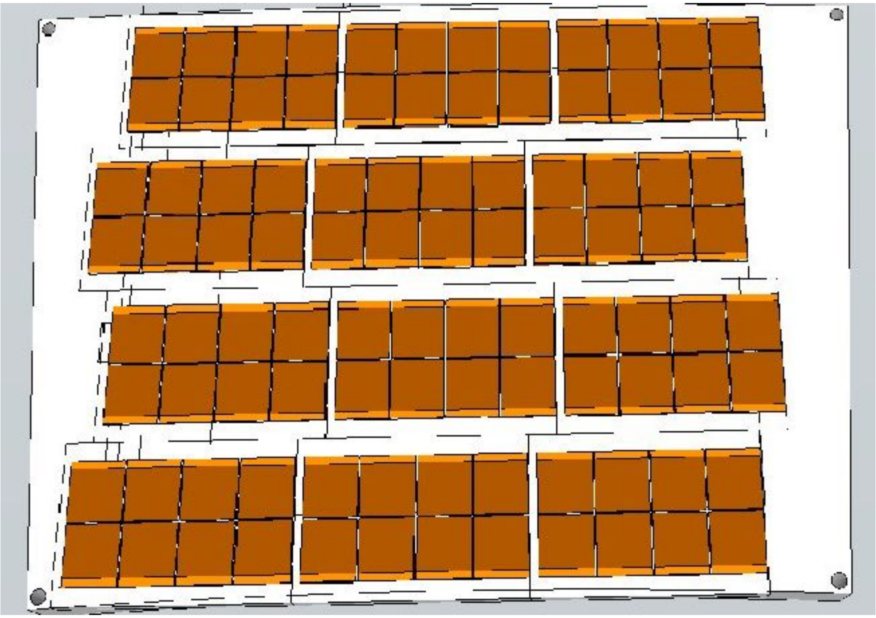
- InGrids show an excellent energy resolution.
  They can easily achieve gas gain ~10000.
- Mass production on wafer scale is available.

- SRS for pixelated TPC is under development.

- Data has been taken successfully at LCTPC LP at DESY
  Analysis is ongoing.

# Outlook

- Timepix3 is coming with many improvements
- SRS based readout system will be extended for larger modules
- 96 chip module for LCTPC LP is in preparation



⇒ bright outlook for a pixel TPC

# Thank you!

LCTPC-pixel:

- CEA Saclay: Andrii Chaus, David Attié, Maxim Titov, Paul Colas
- DESY: Felix Müller, Ralf Diener, Ties Behnke
- NIKHEF: Fred Hartjes, Harry van der Graaf, Jan Timmermans, Rolf Schön, Wilko Koppert
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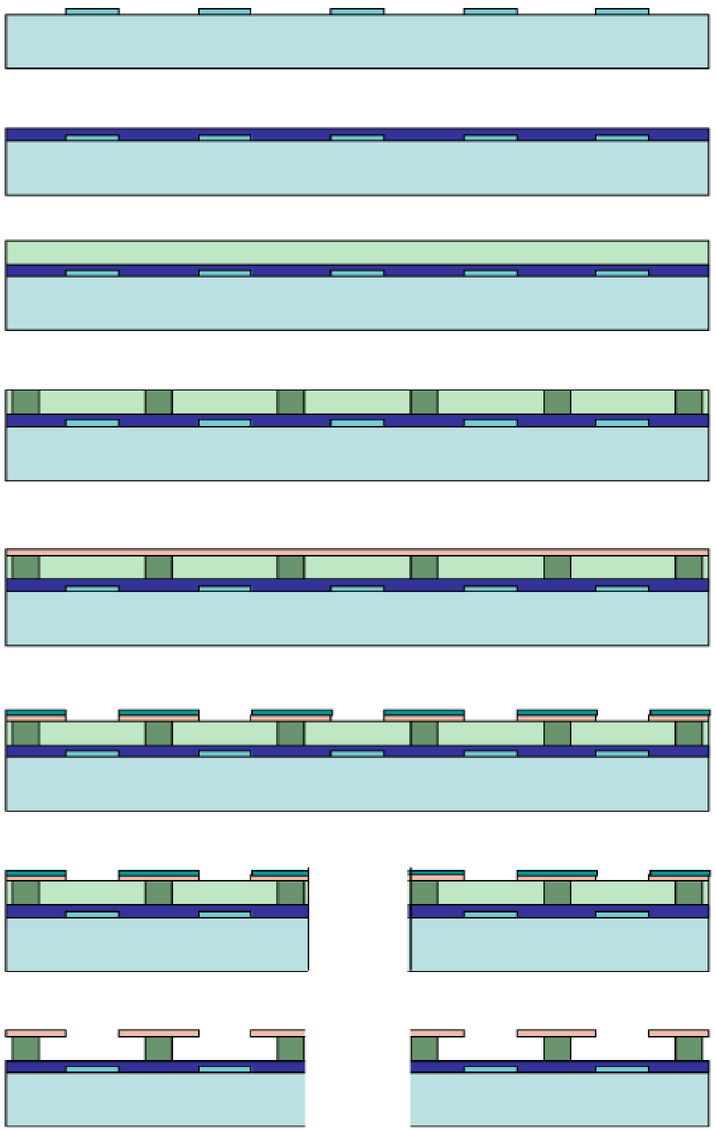
- LAL(Sergey Barsuk), Uni Kiew joining

# Production on wafer scale



1) Probing and cleaning of the wafer
2) Adding $Si_x N_y$ protection layer
3) Application of the SU-8
4) UV-Exposure of the SU-8
5) Application of the grid
6) Patterning of the grid
7) Dicing of the wafer
8) Development of the SU-8

# Data analysis

MarlinTPC & LCIO

Modular Analysis & Reconstruction for the Linear Collider

- Developed within the LCTPC collaboration
- Data processing is highly modular
- Each algorithm is encapsulated in a processor
- Unifed data model LCIO is used
- Sequence and parameter of individual processors are defined in a XML steering file