Status of the InGrid/Timepix activities

48th CAST Collaboration Meeting
Patras

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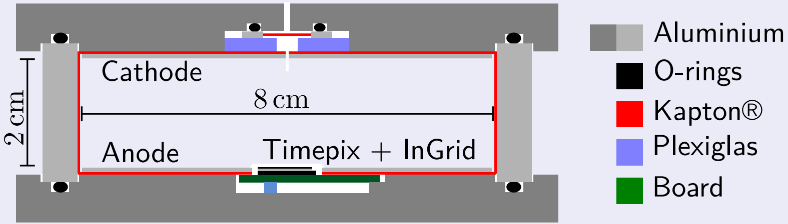
Outline

Detector Concept

InGrid based detector

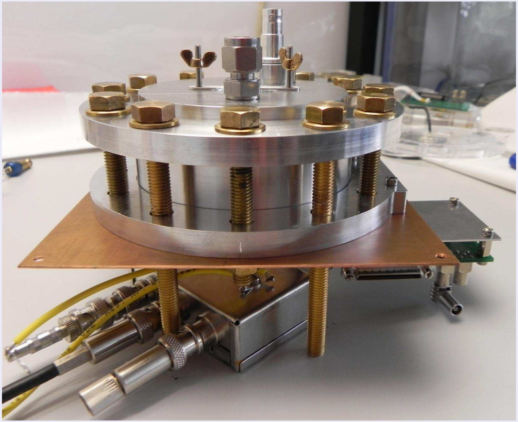


Pixelized Readout

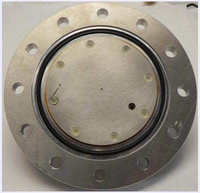
- Detection of single electrons with high spatial resolution
- Energy determination by counting electrons (in principle)
- Possibility to analyze event shape

Current Detector

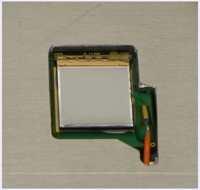
X-ray detector



Cathode



Anode

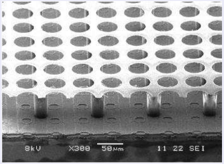


InGrid - Integrated Micromegas

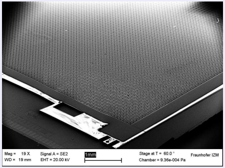
Micromegas on top of Timepix ASIC

- Fabrication by means of photolithographic postprocessing
- Very good alignment of grid and pixels
- Each avalanche is collected on one pixel
- Detection of single electrons possible

InGrid - SEM



Timepix + InGrid



Protection layer

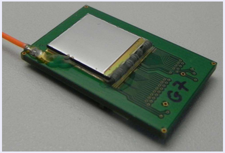
- Timepix was not designed to survive discharges: must protect electronics!
- Resistive layer (2-$8\,\mu\mathrm{m}$ silicon nitride) to spread charge in case of discharge

Timepix ASIC

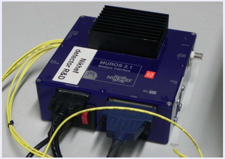
Facts

- 256×256 pixels, $55 \times 55\,\mu\mathrm{m}^2$ pitch
- $1.4 \times 1.4\,\mathrm{cm}^2$ active area
- Charge sensitive amplifier and discriminator in each pixel, $90\,e$ ENC
- Two modes: **Charge** or **Time**

Carrier board



MUROS 2.1

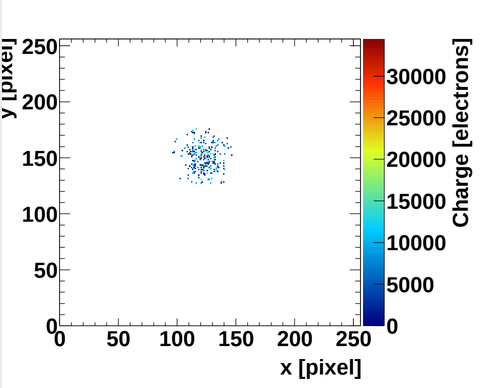


Readout

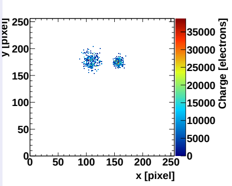
- Readout with **MUROS 2.1**
  Medipix re**U**sable **R**ead**O**ut **S**ystem
  developed at NIKHEF
- Acquisition and control: `Pixelman`

Typical X-ray Events

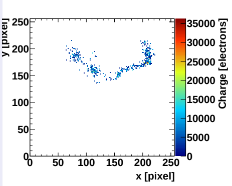
X-ray event



Double event

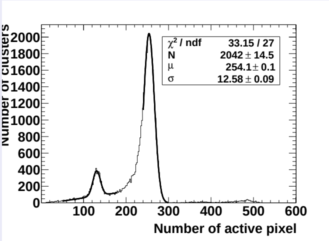


Background event

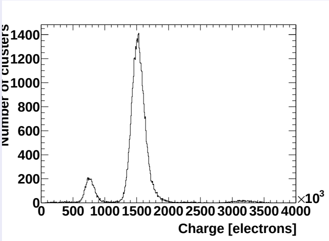


Energy Resolution

Spectrum - Pixels



Spectrum - Charge



Energy resolution

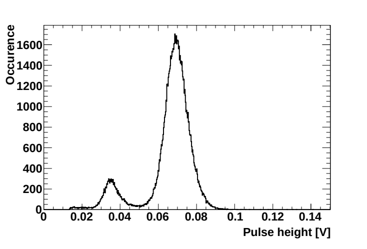
- Energy resolution: $\sigma_N/N \approx 5\,\%$ at $5.9\,\mathrm{keV}$
  Chromium foil to suppress $6.5\,\mathrm{keV}$ line of ^{55}Fe
- Charge spectrum: $\sim 6.6\,\%$ energy resolution
- Gas gain ~ 6500 at $350\,\mathrm{V}$

Decoupling of the Grid Signal

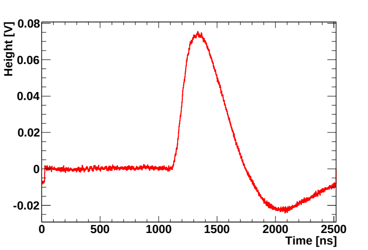
Recording

- ALEPH preamplifier
- CAEN FADC 12-bit $2\,\mathrm{GHz}$

Spectrum - Grid



Grid signal

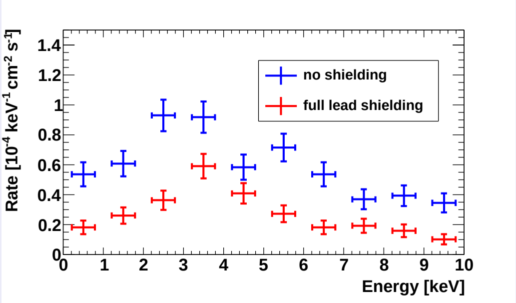


Energy resolution

- $\sigma_E/E \approx 8\,\%$ at $5.9\,\mathrm{keV}$

Background Rates

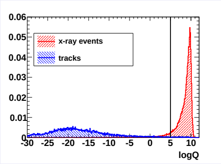
After Likelihood-Ratio based discrimination



- Does software efficiency drop down for low energies?

Lead shielding

Likelihood-Ratio



Work in Progress / Next Steps

Sensitivity at low energies

- α-source plus thin films to get florescence photons
- Need to borrow 'open' α-source from neighboring institute

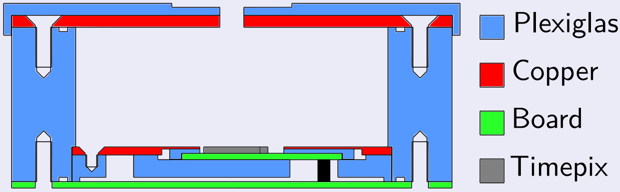
Background suppression

- Improve discrimination algorithm
- Check software efficiency at low energies
- Check activity of lead shielding

New detector

- Assemble it and take it into operation
- Combine readout of Timepix and grid signal (far future)

New Detector Design



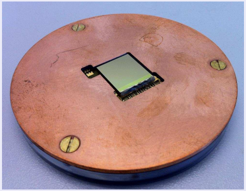
Changes in detector design

- New design based on the CAST Micromegas
  $\rightarrow$ mechanical CAST compatibility
- Plexiglas instead of aluminium
- Metalized Mylar® film ($5\,\mu\mathrm{m}$) as cathode and window
- New carrier and intermediate boards (HV connection from downside, HV feedthroughs, plug and socket connection)

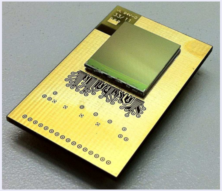
New Detector Design

Drift volume

Readout block



Carrier board



Status

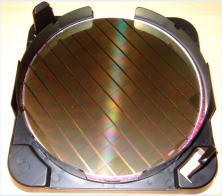
- Received parts from mechanical workshop
- Still waiting for new intermediate board (detector end plate)
- As soon as board arrives and is assembled detector can be put together

Wafer Scale InGrid Production

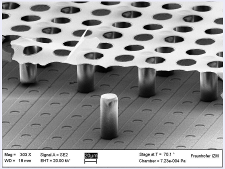
InGrid fabrication

- Fabrication steps take about one week
- Single and few chip processing: NIKHEF / Mesa+ (Twente)
- Wafer processing (~ 100 chips at once): in cooperation with IZM Berlin

Timepix wafer



IZM InGrid - SEM



Results of wafer processing

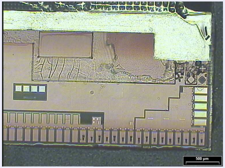
- Structures of IZM InGrids look and behave good (similar to Twente InGrids)
- **BUT:** chips die fast when operated above moderate grid voltages & some inactive (less sensitive) areas

Wafer Scale InGrid Production

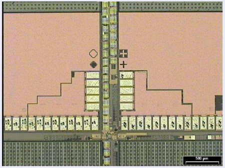
Formation of the protection layer

- Vapor deposition process
- Very critical, high temperature ($> 200\,^{\circ}\mathrm{C}$)
- Bondpads have to be protected
- Achieved with photolithographic polyimide mask and a lift-off process

Covered bondpads



Clean bondpads

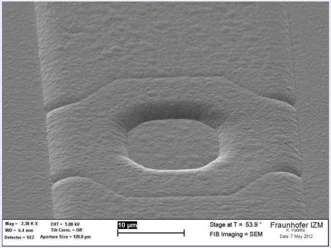


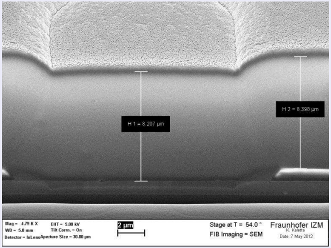
How to solve the 'issues'?

- Inactive areas: probably residuals from cleaning → improve cleaning procedure
- Dieing chips: several possible reasons (e.g. cracks in protection layer) → Investigation is ongoing

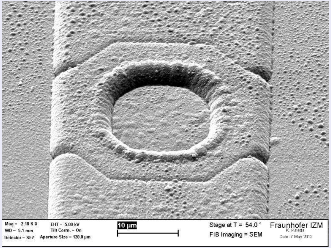
Focused Ion Beam Imaging

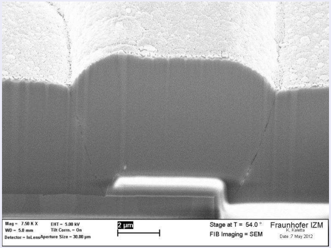
Twente InGrids





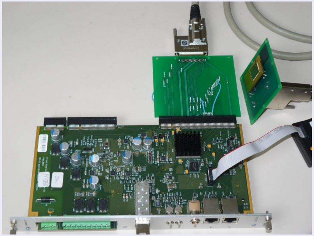
IZM InGrids





Scalable Readout System - SRS

Prototype readout



Why do we need a new readout?

- MUROS is no longer produced
- MUROS is quite slow and inflexible

Scalable Readout System

- FPGA based, very flexible
- Needed for Timepix readout: Custom FPGA firmware & custom adapter board

Benefits

- Up to $70\,\mathrm{Hz}$ readout frequency ($\sim 10\,\mathrm{ms}$ dead time)
- Usage of grid signal as 'trigger' should be possible

Conclusion & Outlook

Conclusion

- Grid signal could be recorded successfully
- New detector will be available soon, so tests can start
- Tests with low energy photons should be possible soon
- InGrid production on wafer scale works in principle
- New readout system for the Timepix is under development
- Still much work to do ☺

Outlook

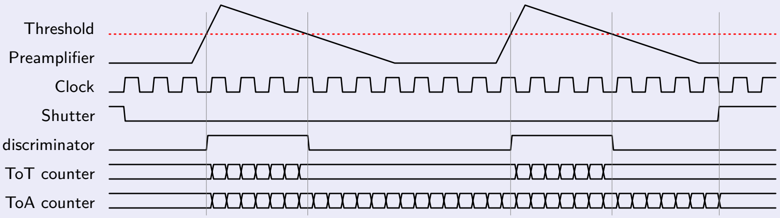
- Test data-taking at CAST or at least at the CAST area towards end of the year

So long, and thanks for all the fish. . .

Backup

Timepix ASIC

Timing Diagram



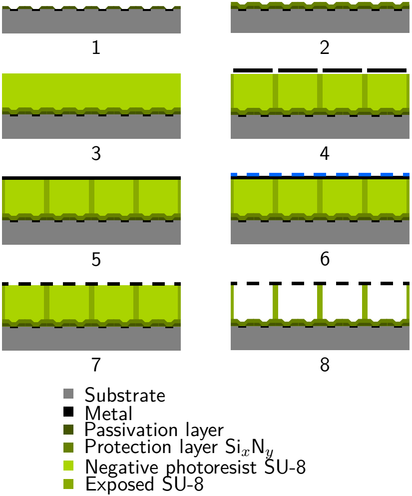
Timepix 3

- Is under development and will be submitted this year
- Will be able to recognize multihits and to measure ToT and ToA simultaneously
- Will allow data driven readout

Fabrication of an InGrid

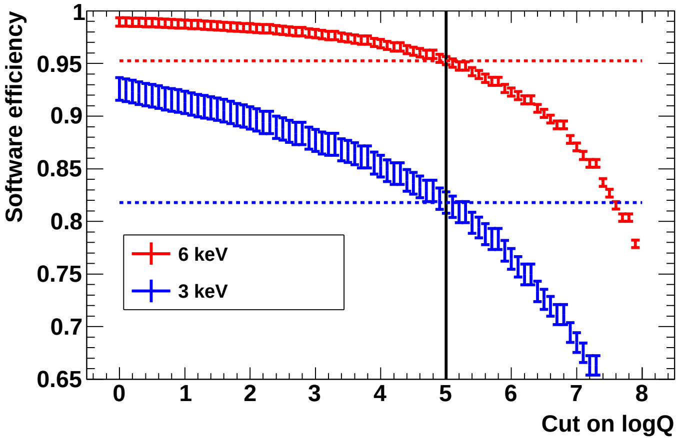
Fabrication steps

1. Starting with bare Timepix
2. Deposition of protection layer ($8\,\mu m$ Si_xN_y)
3. Deposition of negative photoresist SU-8 ($50\,\mu m$)
4. Exposure of SU-8
5. Sputtering aluminium
6. Putting mask on aluminium layer (photoresist)
7. Structuring aluminum layer
8. Development of SU-8, cleaning of interistitials



Background suppression

Software efficiency



Background suppression

Background rejection