Ethernet-driven readout system for gaseous detectors

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Kick-Off meeting, CERN 16-18 February 2011, WP9

Outline
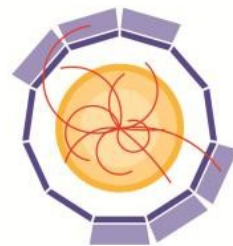
Subtask 9.2.3 (CEA, Mainz, Bonn, NIKHEF): Common readout systems for gaseous detectors. Auxiliary electronics for the read-out of pixellated front-end chips, aimed at highly granular pixel read-out of gas detectors, are to be developed.
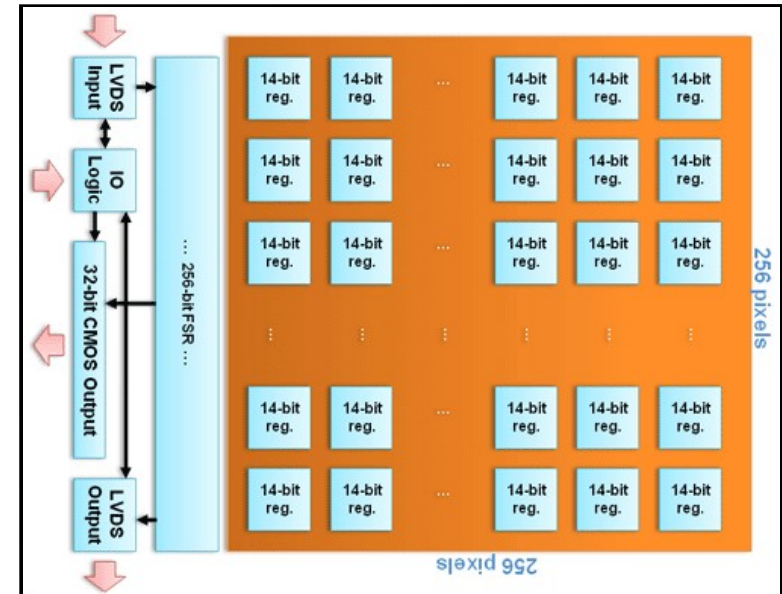
- Timepix Chip
- Current MUROS readout system
  - Single chip readout
  - Multi chip readout
- New readout system
  - First steps
  - Status
  - Way to go
- Timepix2

Introduction: The Timepix Chip

- Characteristics:
  - 1.4 x 1.4 cm²
  - matrix of 256 x 256 pixels
  - 0.25 µm CMOS technology (33 M transistors/chip)
  - 55 x 55 µm² per pixel
  - serial or parallel I/O (readout time less than 300 µs)
  - preamplifier/shaper (rise time ≈ 90-180 ns)
  - discriminator
  - 14-bit counter
  - minimum detectable charge: ≈ 650 e-
  - using GEM or Micromegas (InGrid) as amplification structure

Introduction: The Timepix Chip

- TOT mode: Charge counting
- Time Mode: measuring the arrival time
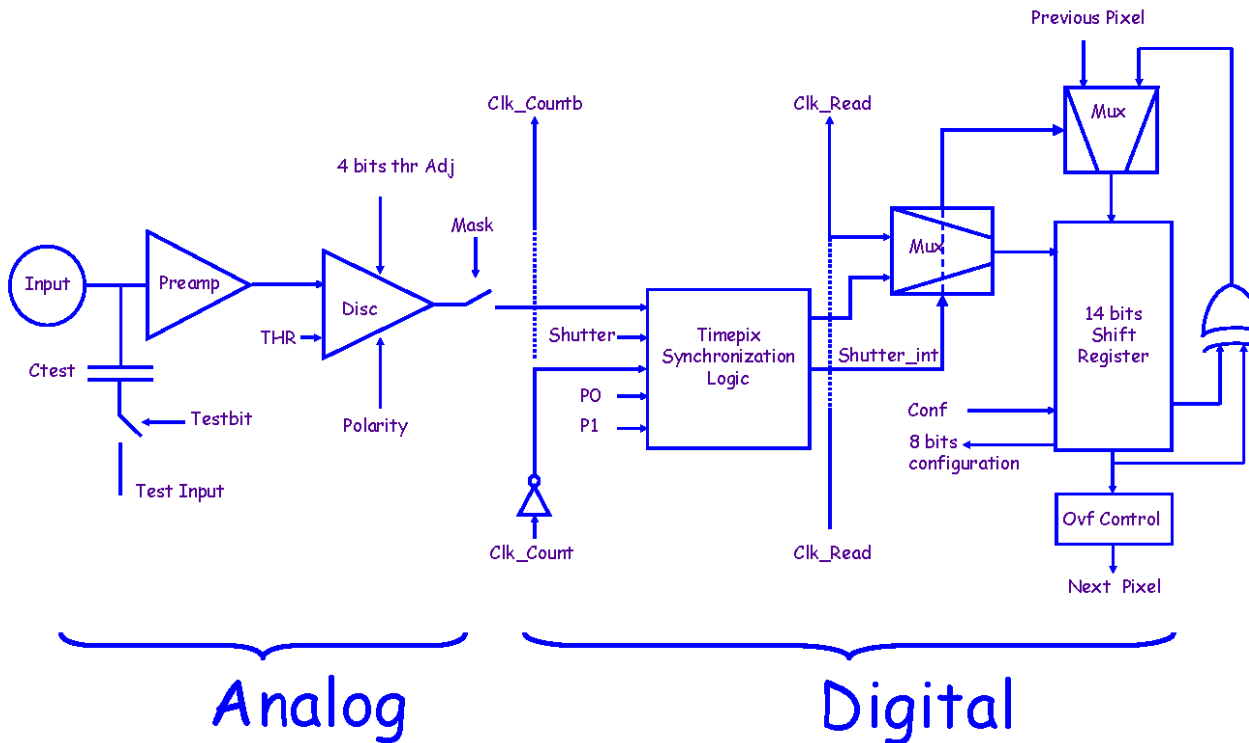
MUROS readout system

- MUROS v2.1:
  - designed at NIKHEF for Medipix2 and Timepix chip readout (new FPGA code)

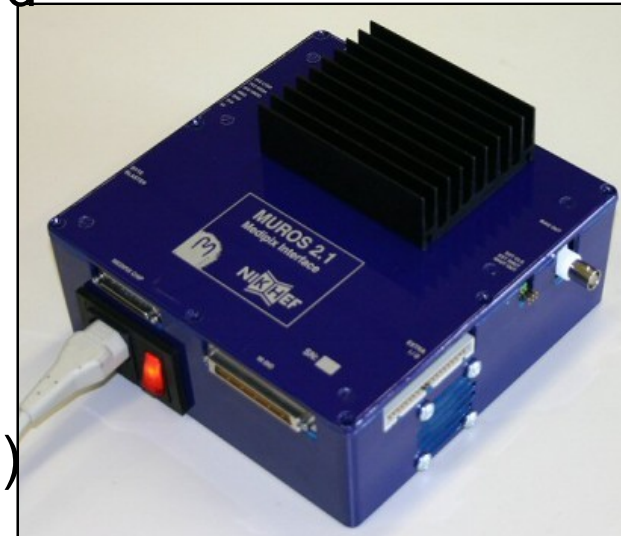 - serial readout for at most 8 Timepix chips
  - VHDCI cable <3 m to Timepix carrier board
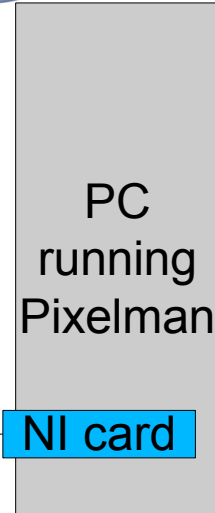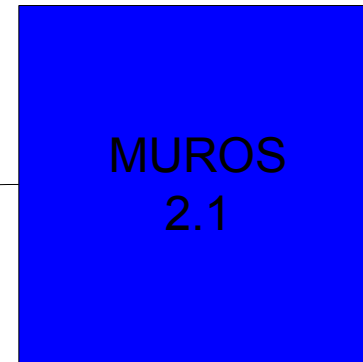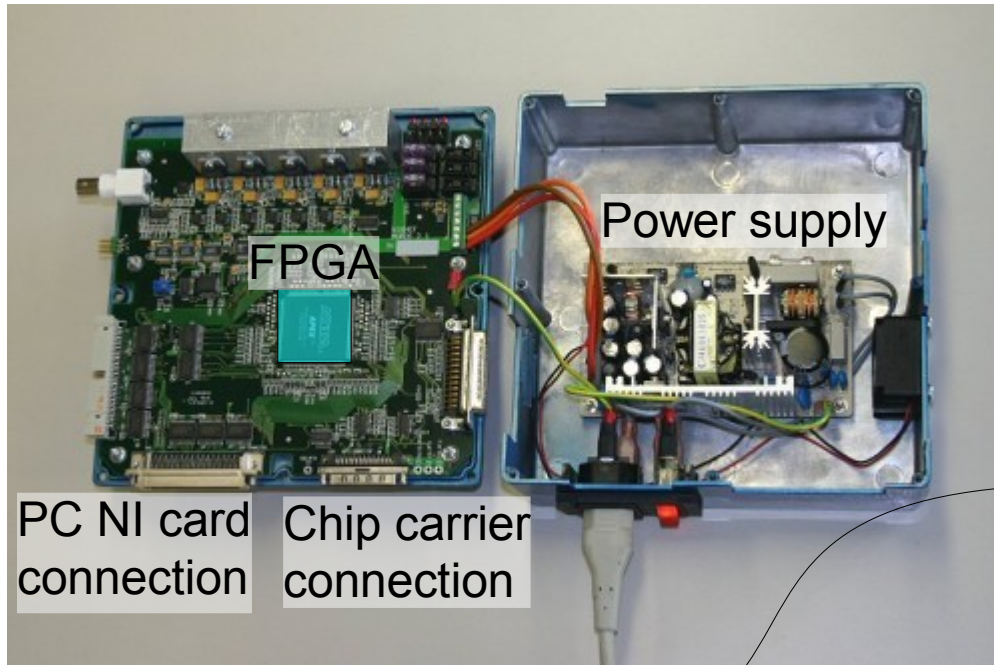 - VHDCI cable to NI card in PC
  - Timepix readout: theo. < 50 frames/sec lowered by shutter length
  - adjustable readout frequency [<240MHz]

  - data acquisition on PC(Pixelman software)

http://www.nikhef.nl/pub/experiments/medipix/muros.html

MUROS readout system
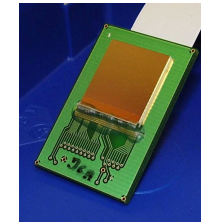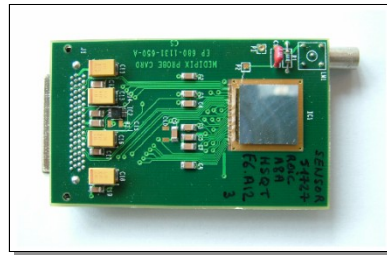

- Problems with MUROS v2.1:
  - only limited availability, no production
  - NI card and driver out of date
  - at most 8 chips daisy chained
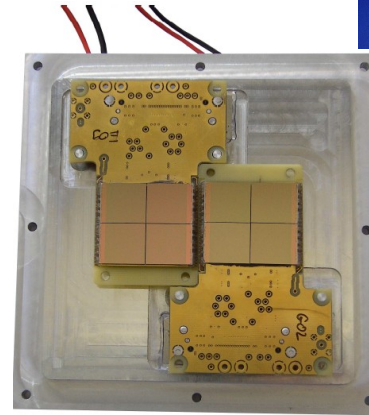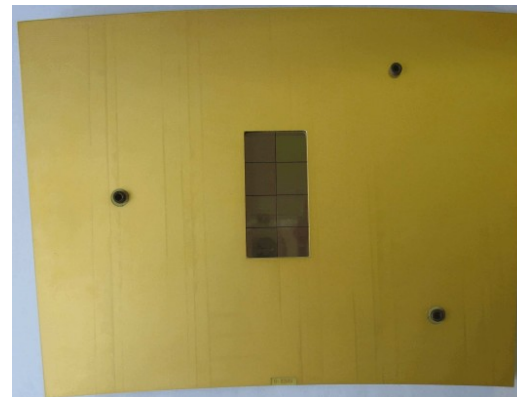
Timepix carrier boards

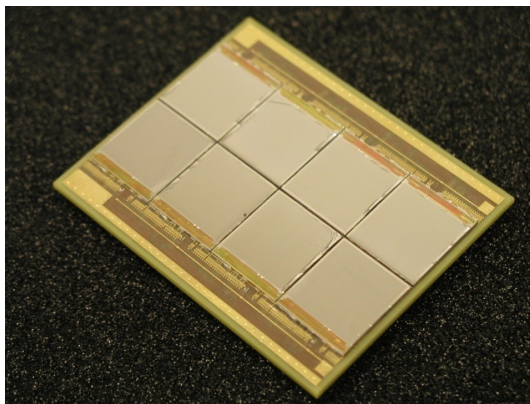- Single chip

- NIKHEF quad board

- Saclay 8 chip InGrid panel „Octopuce" for LP TPC
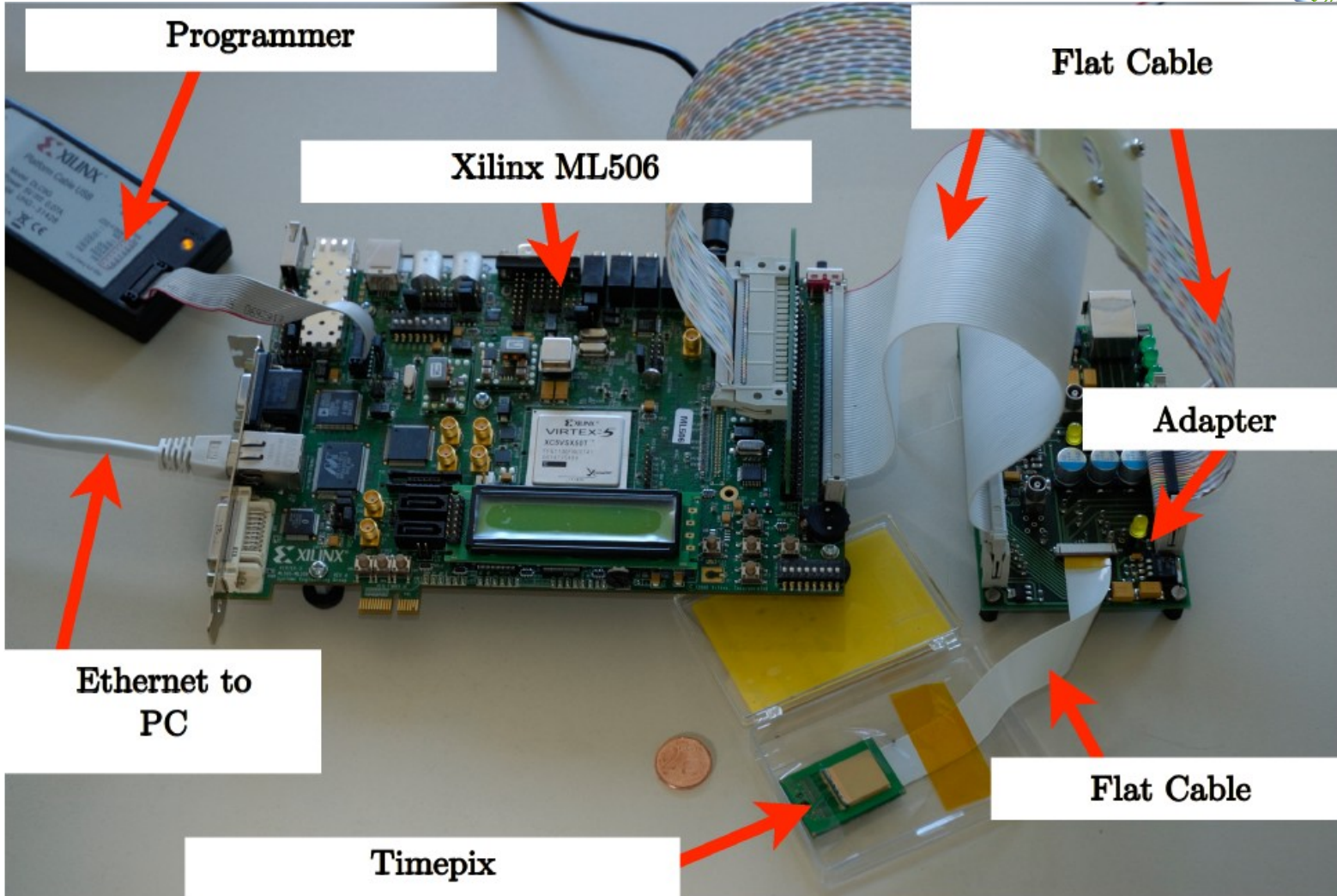
New readout system

- Goals:
  - ultimately read out ~100 chips
    - → large area detector (e.g. full LP module)
  - modular system → use SRS (RD51)
  - ethernet based
  - use Virtex6 FPGA
  - zero suppression
  - Triggerable, integrate with slow control & calibration
  - Timepix2 compatibility in view

First steps

- Single Chip readout (Uni Mainz)
  - Timepix chip on FR4 carrier
    - LVDS link
  - Adapter board
    - trigger
    - test pulses
    - power supply
  - Xilinx ML506 evaluation board (Virtex5)
    - Timepix control
    - ethernet (UDP) communication
  - PC software
    - command prompt based
    - Timepix control
    - data acquisition

Programmer

Flat Cable

Xilinx ML506

Adapter

Ethernet to PC

Flat Cable

Timepix

Adapter board

FPGA
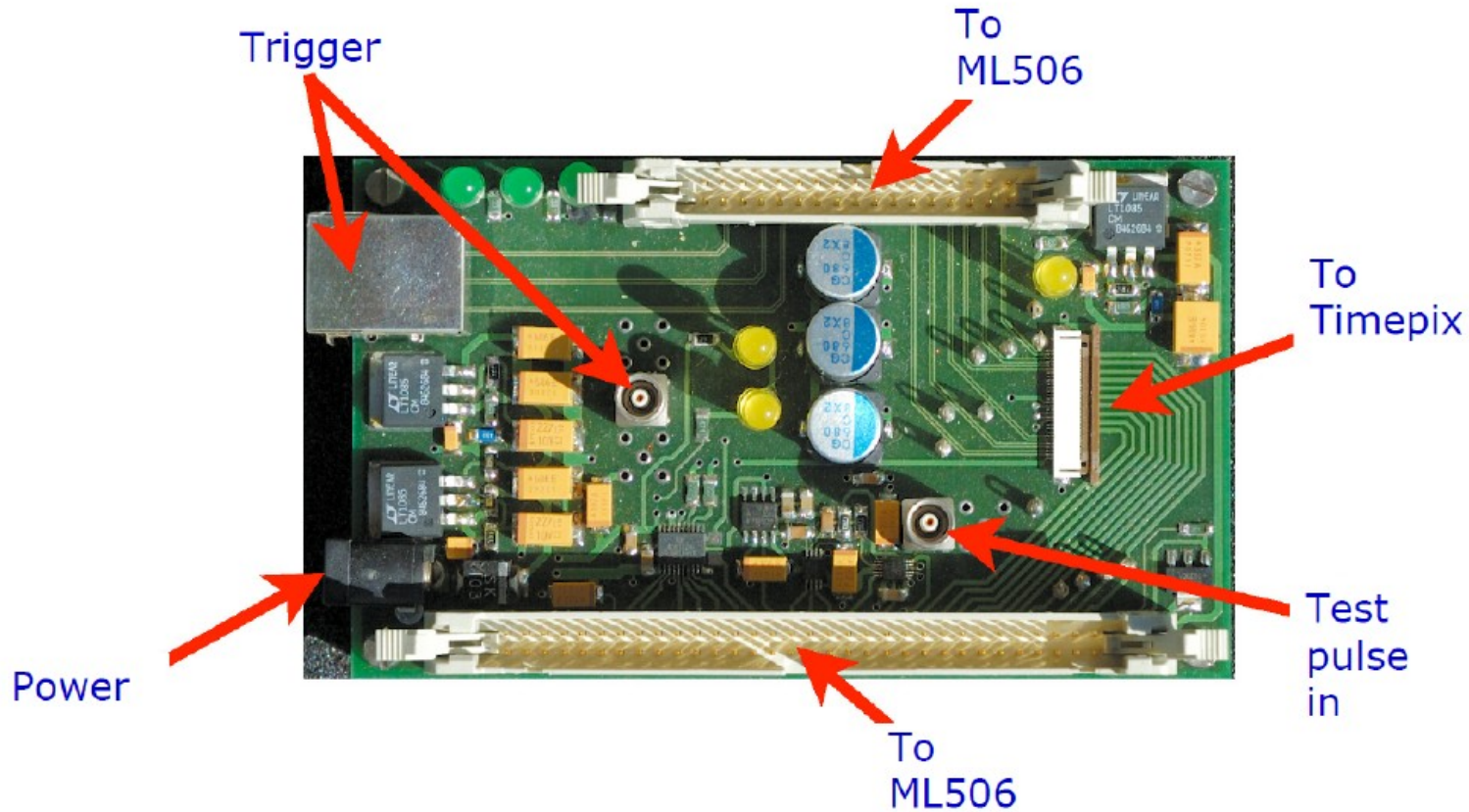
- On-chip Ethernet MAC
- On-board Gigabit Ethernet phy chip
  - 1000BASE-T
  - no embedded CPU
- Firmware
  - VHDL description
  - Common clock for digitisation and data transfer, crystal based
  - Serial/deserial interface to the Timepix bit-serial port
  - Timepix matrix data not buffered n FPGA
    $\rightarrow$ kept on Timepix while awaiting packet transmission
  - Shutter with programmable delay and width
    - software control or
    - external trigger (TLU)
 - Non-volatile storage of hardware description on CF card

PC Software

- C++ with Qt
- Command line interface, GUI will be developed (Mainz)
- Data pulled by computer (handshake)
- Minimal network protocol stack
  - ‹ethernet›‹IP›‹UPD›‹control›‹data›
  - standard ethernet/IP/UDP headers

- Functionality:
  - reset, setup (Timepix mode, matrix mask, DAC settings) shutter, readout, test pulse enable, choose trigger
  - start a run: set FSR, set matrix, readout matrix setup, DAQ
  - threshold adjustment under way

Test and Results

- Lab test in Mainz: Timepix readout
- Run with TPC in Bonn
  - event rate up to 55.5 Hz @ 100 MHz
  - improvement to MUROS2, but lower than expected
  - bare Timepix chip would be ≈ 100 Hz (using LVDS link)
  - data pipelined through FPGA, no noticeable latency, low packet overhead
  - bottleneck probably due to latency in Linux IP stack

p=256*256*14+256+8
h=64*8
n=p/1024
f(x) = 1 / ((p+h)/x + n*l)
   => l=10.2e-6
g(x) = x / (p+h)
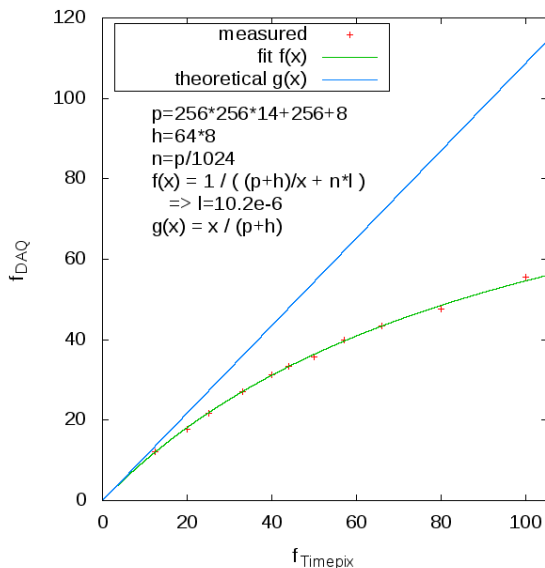
$$\Rightarrow f_{\text{DAQ}} = \left(n \cdot \left(\frac{\text{payload} + \text{header}}{f_{\text{timepix}}} + \text{latency} \right) \right)^{-1}$$

f_{timepix}: operating frequency (variable 12.5 - 100 MHz)

n: number of packets

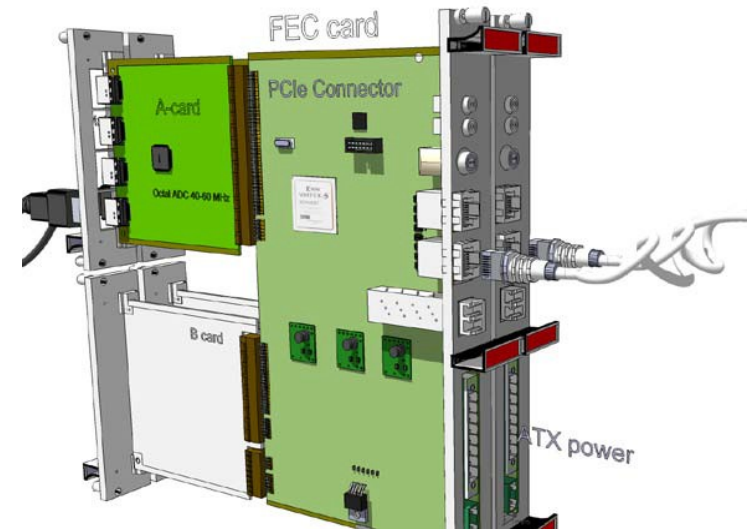universität **bonn**

Bonn activities starting:

- Setup of second Mainz system in Bonn ✓
  - Xilinx ML506 board Virtex5 FPGA
  - single Timepix readout
  - adapter board
- Re-target to Virtex6
  - Xilinx ML605 board with Virtex6 FPGA ✓
  - firmware modifications to Virtex5 VHDL
    - new ethernet MAC ✓
    - adapt to different clock and pin setup ✓
    - implement timepix control moduls ✓
    - solve timing problems
  - hardware modifications
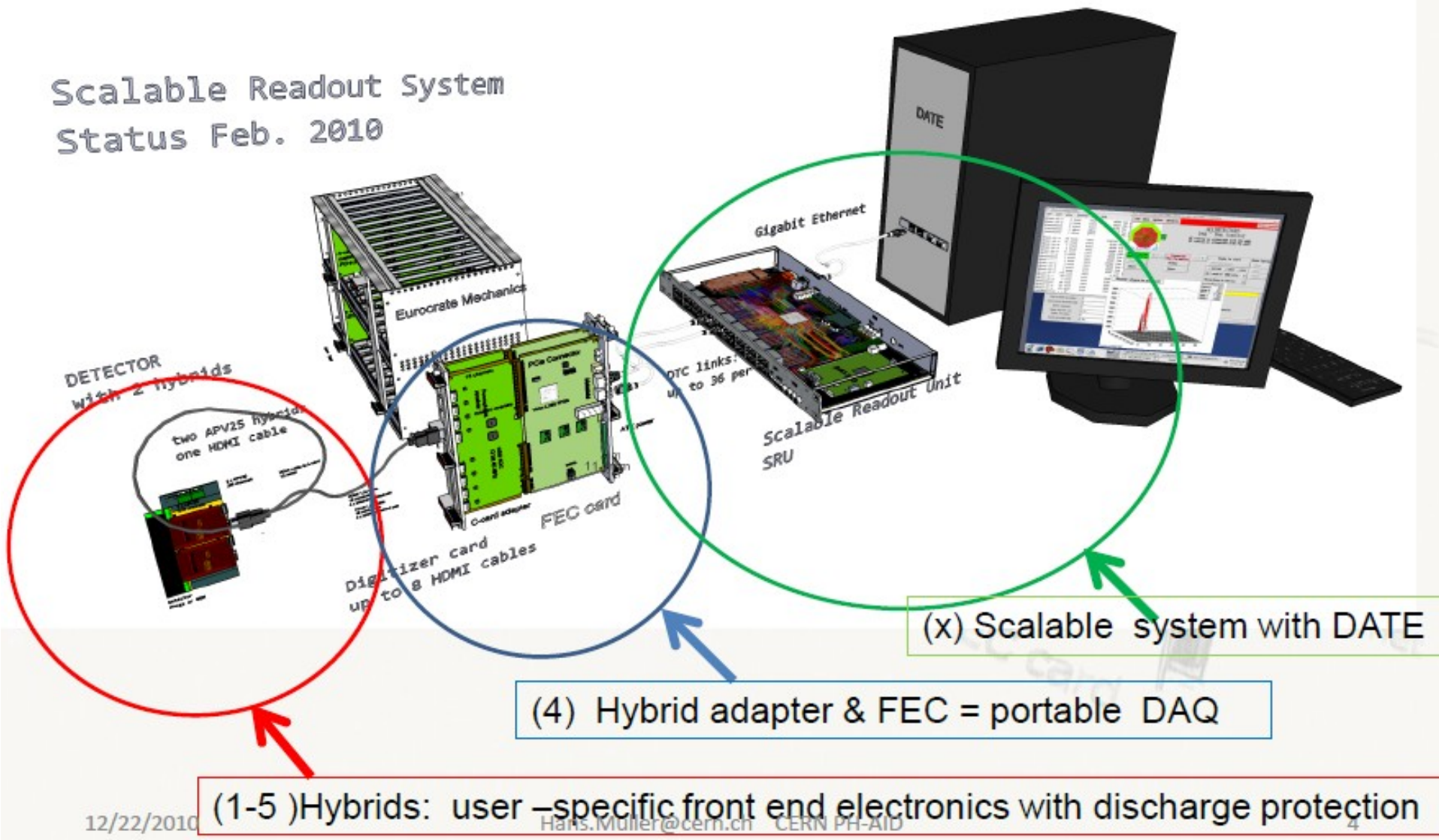   - adapter board for cabling

Way to go

- Advancement of PC software (Mainz)
- Multi chip (first step: 4 or 8) readout with Virtex6 (Bonn)
- Mechanics of box to house Readout card, including all connectors, supplies, switches and LEDs (Saclay)
- Modular system: Scalable Readout System SRS:
  - small set of modular components
  - performance at low cost
  - designed for scalability
    (e.g. 1 FEC for 8 chips x
    14 FEC/crate = 112 chips)
  - plugin-choice of frontend ASICs
  - open developer platform
    for physics algorithms
  - supported software made for physics
  - Developed at CERN for RD51

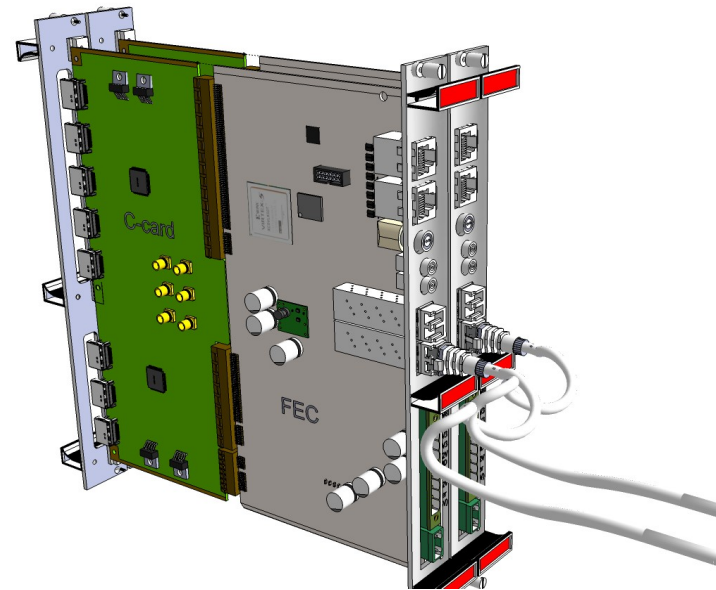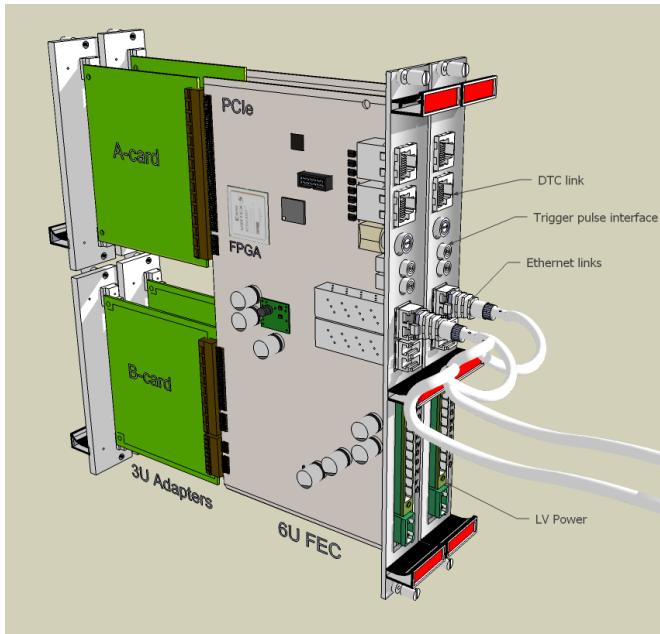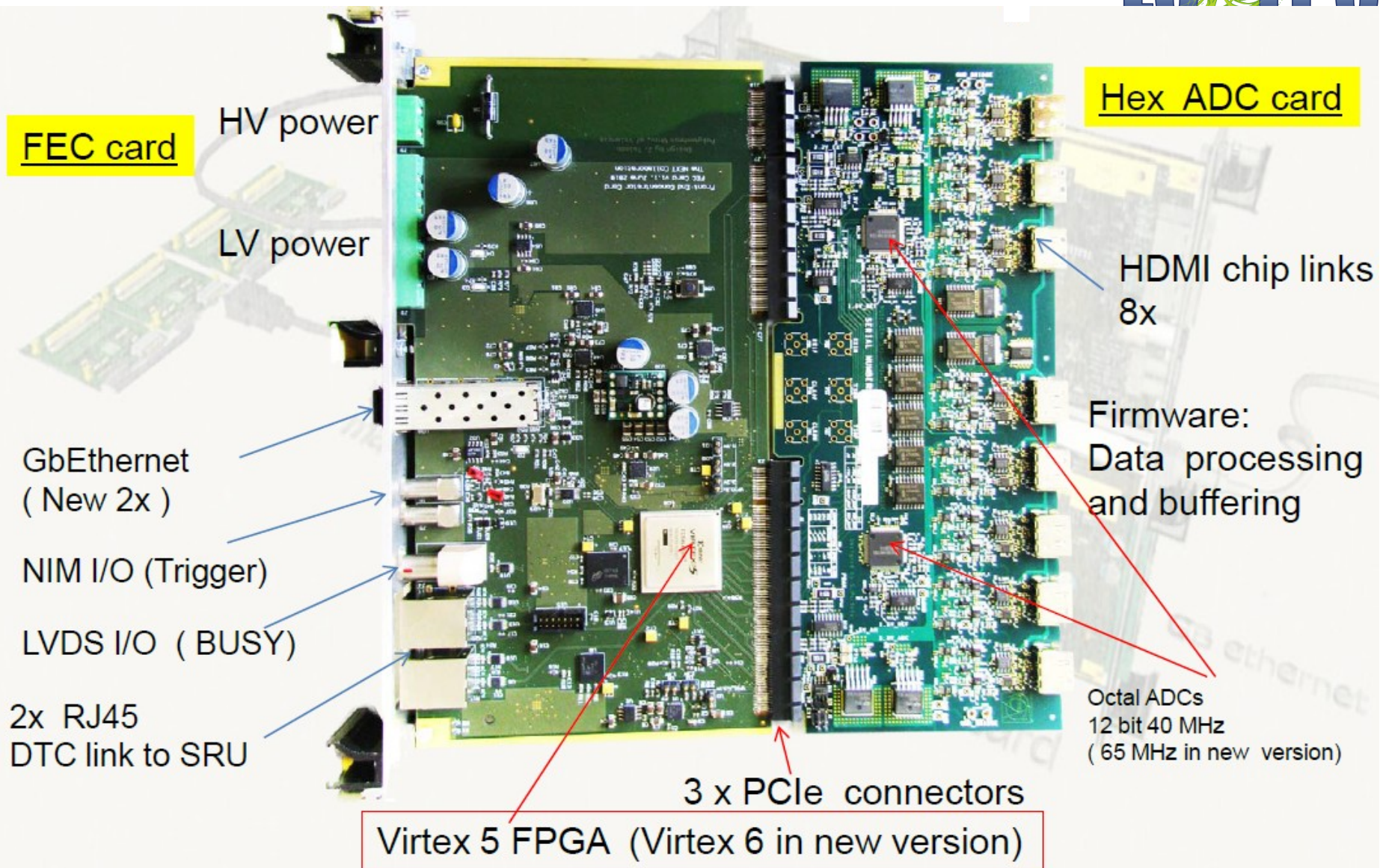Scalable Readout System
Status Feb. 2010

DATE

Gigabit Ethernet

Eurocrate Mechanics

DETECTOR
with 2 hybrids

two APV25 hybrids
one HDMI cable

PCIe Connector

FEC card

C-card adapter

Digitizer card
up to 8 HDMI cables

DTC links:
up to 36 per

Scalable Readout Unit
SRU

(x) Scalable system with DATE

(4) Hybrid adapter & FEC = portable DAQ

(1-5)Hybrids: user –specific front end electronics with discharge protection

FEC and adapter cards

- A –Cards: 4 U
- B –Cards: 4 U for miscellaneous extensions and LV-HV control
- C –Cards: 8 U

FEC and C-size ADC adapter

FEC card

HV power

LV power

GbEthernet
(New 2x)

NIM I/O (Trigger)

LVDS I/O (BUSY)

2x RJ45
DTC link to SRU

Hex ADC card

HDMI chip links
8x

Firmware:
Data processing
and buffering

Octal ADCs
12 bit 40 MHz
(65 MHz in new version)

3 x PCIe connectors

Virtex 5 FPGA (Virtex 6 in new version)

Timepix2 Chip

- Medipix-3 collaboration has decided to design Timepix2
- Improvements: (to Timepix)
    - 130 nm technology (250 nm)
    - 1.7 ns time binning with 600 MHz local oscillator (>10 ns)
    - external trigger system
    - On-chip zero-suppression, fast output links
    - TOT and Time information in each pixel
    - minimal dead time
    - through-silicon-via capable

Summary

- Timepix chip (single, quad, octo) is used as readout structure in gaseous detector (prototypes)
- Current readout system (MUROS2) can handle up to 8 chips
- Largest area covered: 2.8 x 5.6 cm²

- New readout system under development
  - single chip readout realised
  - hardware description for Virtex6 FPGA
  - a scalable readout system to handle ~100 chips is aimed for
  - SRS will be used with Timepix2 chip
  - Readout for large area gaseous detector

Thanks to Christian Kahra (Mainz) and
Hans Müller (CERN,SRS) for their slides

Backup slides

Hardware
The Timepix Chip

A modified MediPix2 Chip for TPC applications
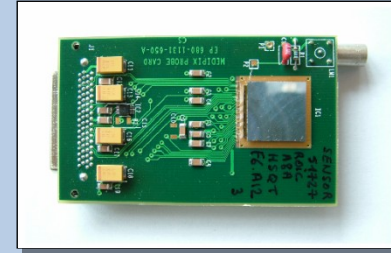
Characteristics :

- 1,4 x 1,4 cm²
- matrix of 256 x 256 pixels (CMOS, IBM)
- 55 x 55 µm² per pixel
- Preamplifier/shaper (t_{rise} ~150 ns)

Motivation: knowing the time of arrival of avalanches at pixels
$\Rightarrow$ use 14bits for counting clock cycles

- lower threshold
- clock up to 100 MHz in each pixel
- noise threshold ~ 500 e-
- digital output signal
- 4 different modes possible

Discriminator signal

Medipix mode

TOT mode

TIME mode

1Hit mode

Shutter window
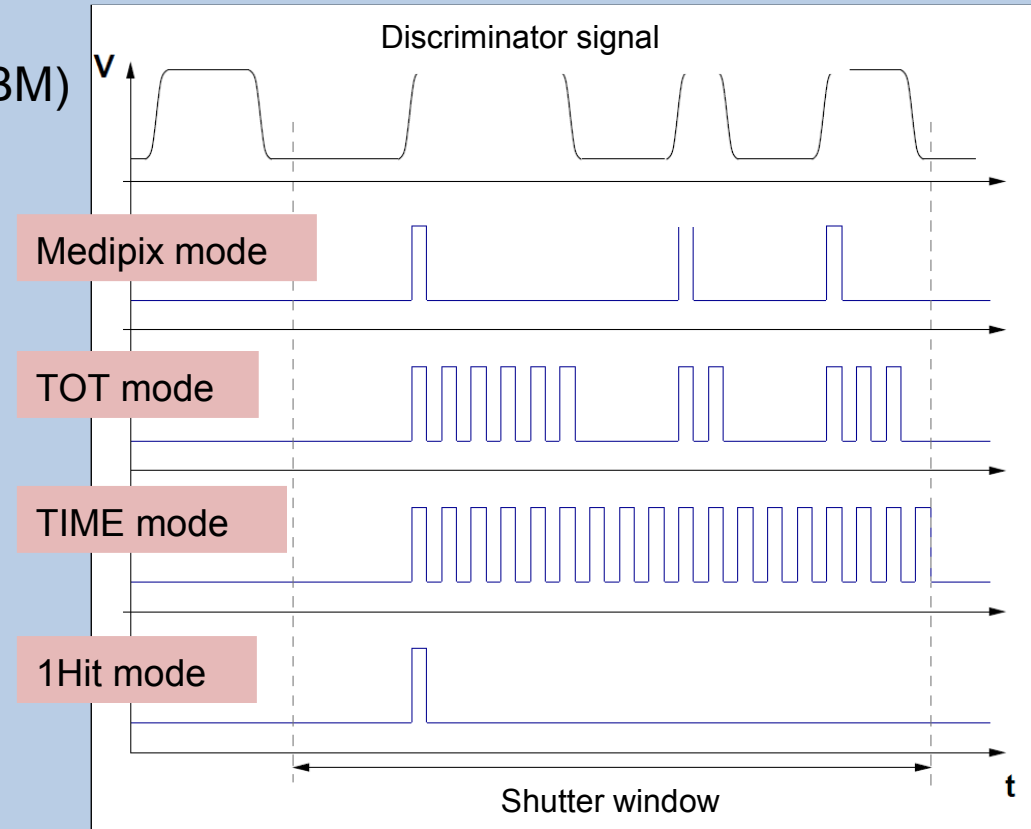
Hardware

Timepix + Ingrid = Pixelated Micromegas

TimePix+Micromegas:

- No alignment between pixels and holes in grid
- pillars visible
- variation of distance between anode and grid
- irregular structure
$\Rightarrow$ Gain inhomogeneities, Moiré effect

Solution:

GridPix: TimePix Chip with Micromegas structure in post-production (photolithography)
- alignment of grid
- flat surface
- regular structure
- possibility to vary grid parameters in post-process

!

8kV   X300   50μm   11 22 SEI

Drift gap

Avalanche

~50 μm
80 kV/cm

Amplification gap
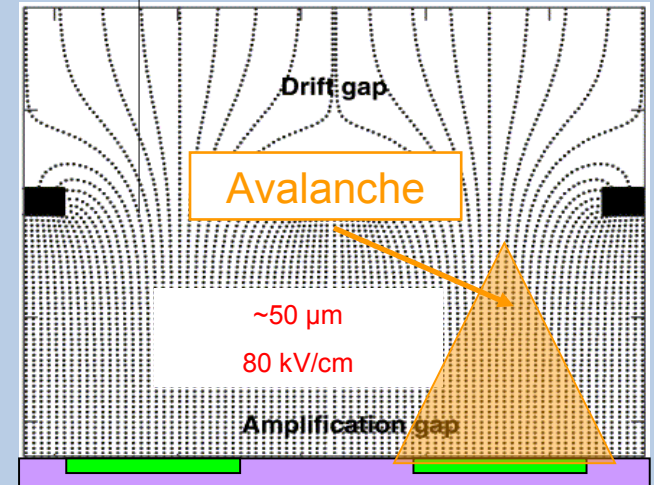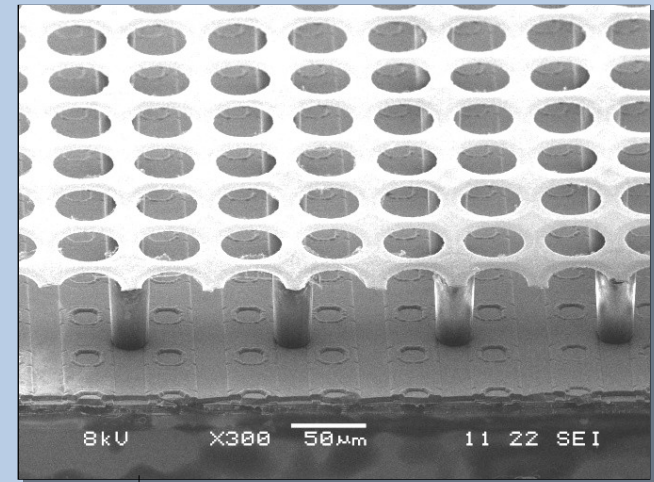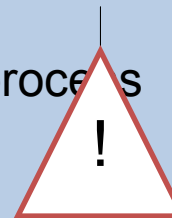
Attention to discharges $\Rightarrow$
place an additional layer: **SiProt**

Hardware
Calibration

$$C_T = 8\,fF$$
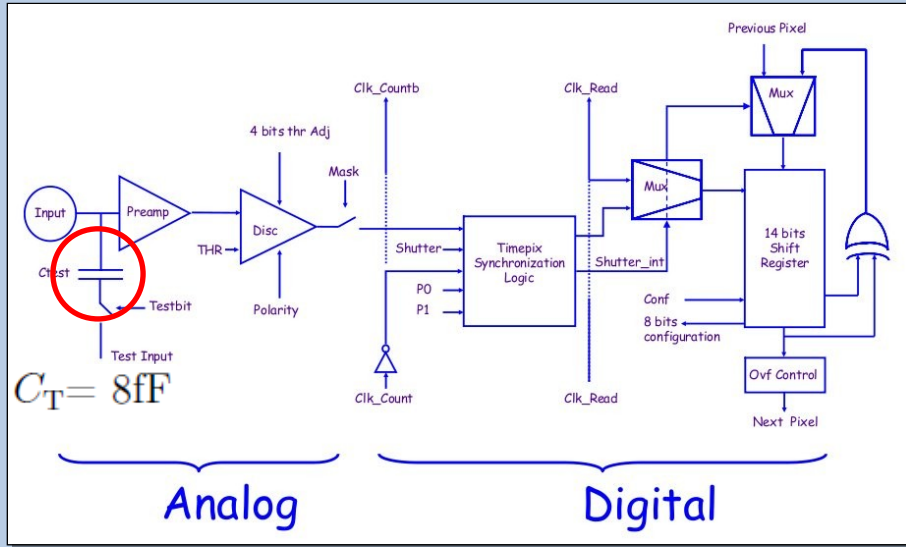
$$Q_{inj}\,[e^-] = 50 \cdot \Delta U_{inj}\,[mV] \qquad Q_{inj} = C_T \cdot \Delta U_{inj}$$

Internal test pulses applied to each pixel via MUROS

→ Known input charge into electronics

→ Threshold calibration
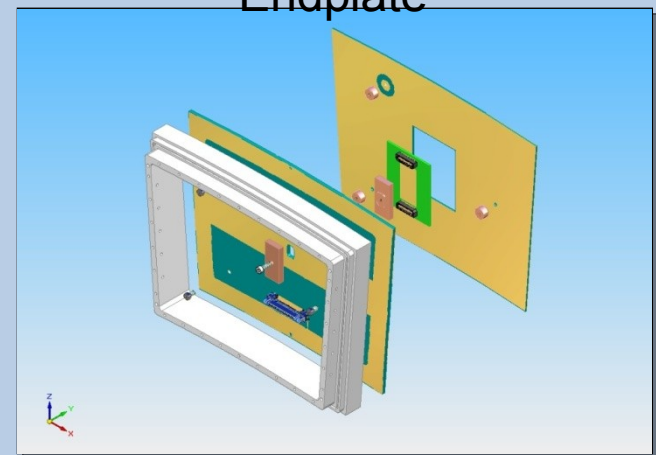→ TOT calibration !Non linear for low charge

Threshold DAC → #e- calibration

TOT → #e- calibration

8 Chip panel
Large Prototype for LC TPC

Aim: A panel with 8 TimePix InGrid Chips for the large TPC prototype
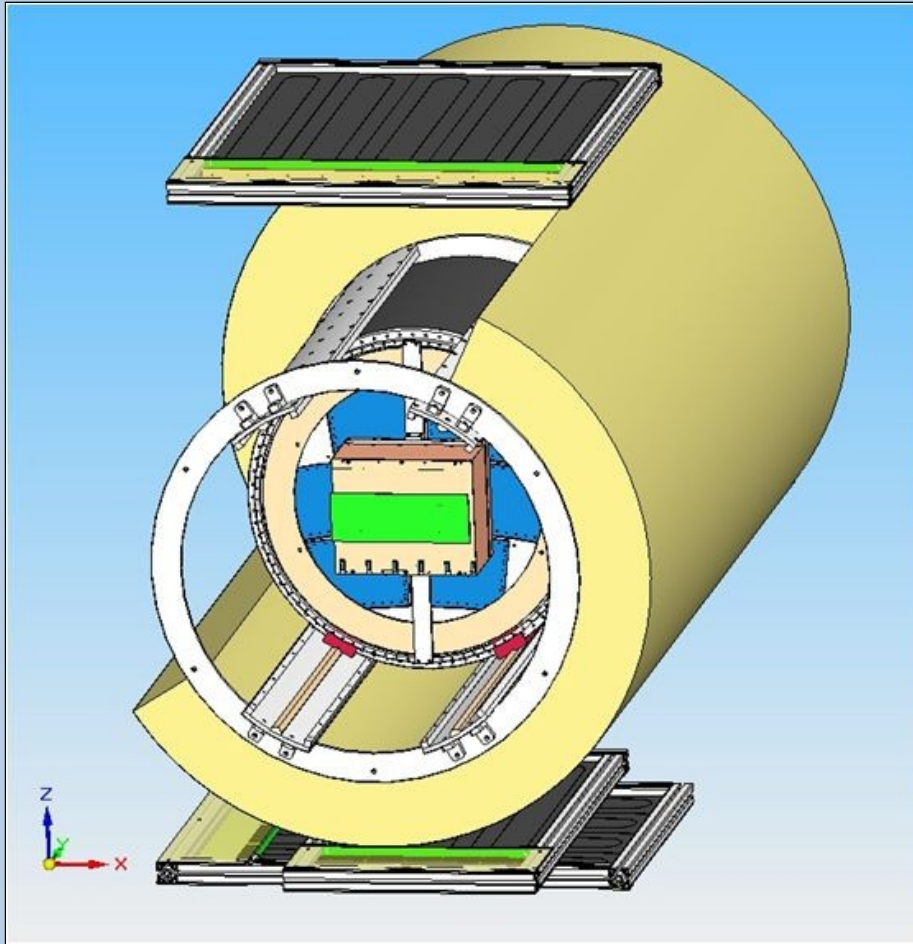
Prototype for LC TPC at DESY
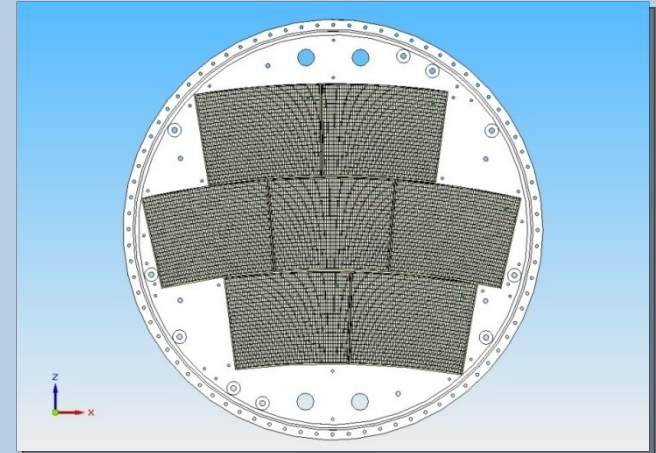
Endplate

One module

8 Chip panel
Octopuce

First equipped with 8
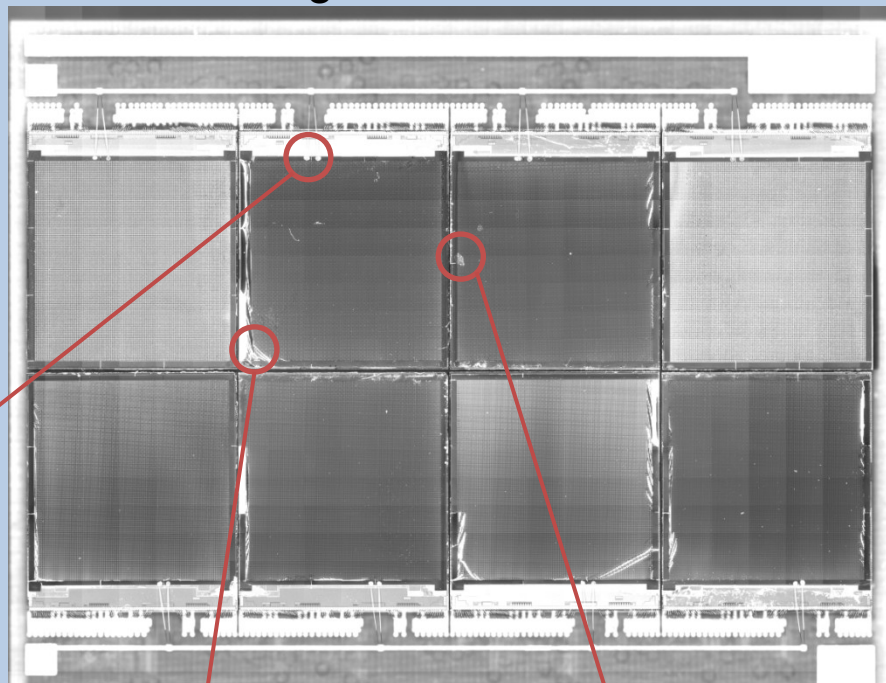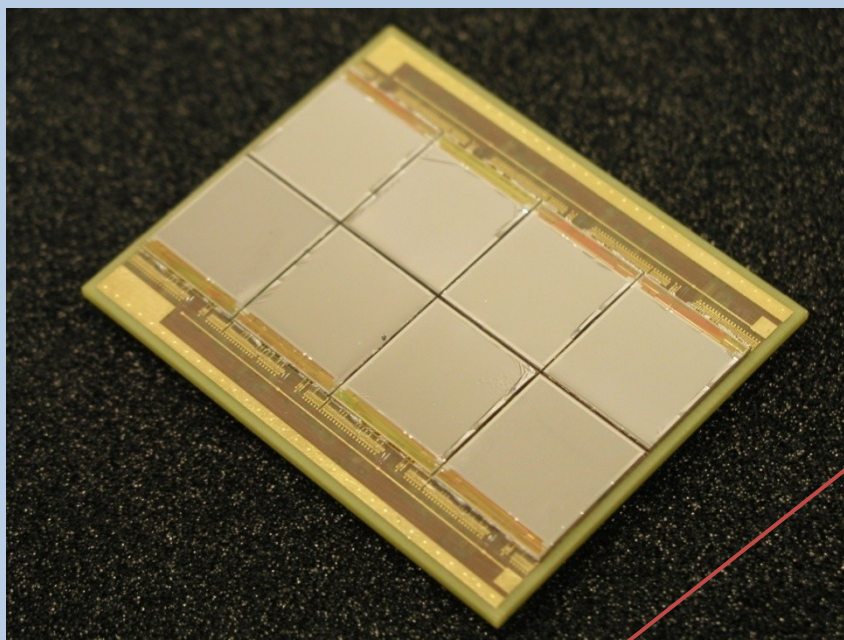naked Timepix chips
in NIKHEF bonding lab
by Joop Rövekamp

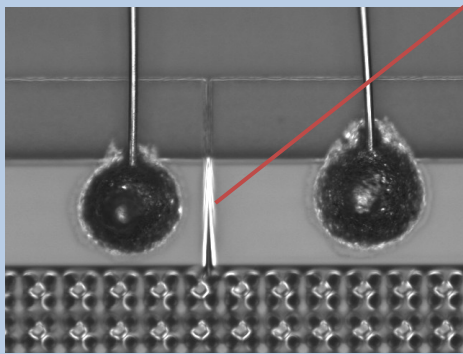⇒to ensure operability
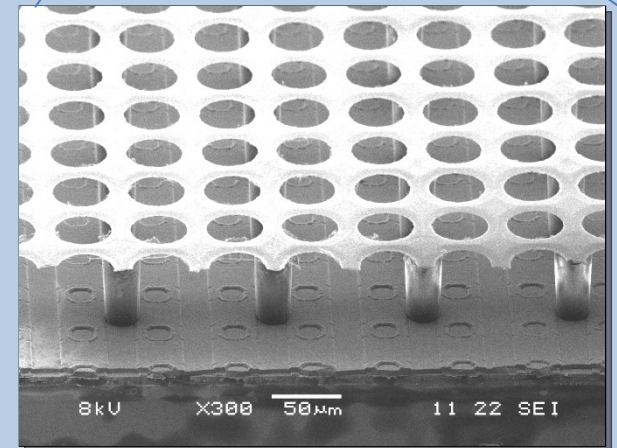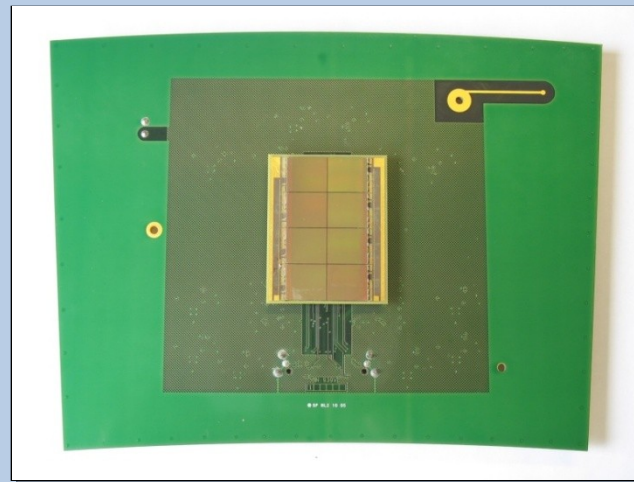
8 Chip panel
Octopuce

29.04.2010: 8 Tempi + Ingrid Chips glued and bonded daughterboard at NIKHEF

Microscope: Grids not perfect, but very good

Grid HV bonds fixed with silver glue