GOSSIPO-3: Measurements on the Prototype of a Read-Out Pixel Chip for Micro-Pattern Gas Detectors

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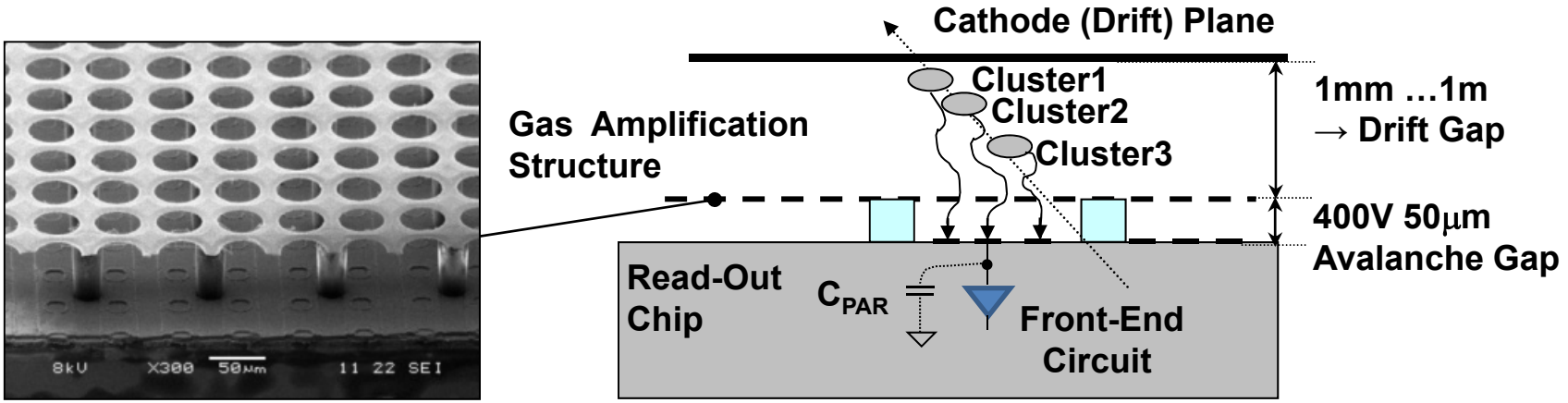
Outline

- Read-Out of Ingrid-Gaseous Detectors
- GOSSIPO-3: Features & Architecture
- Measurement Results & Discussion
- Summary & Outlook

Read-Out of Ingrid-Gaseous Detectors

Gas-avalanche detector combining a gas layer as signal generator with a CMOS readout pixel array

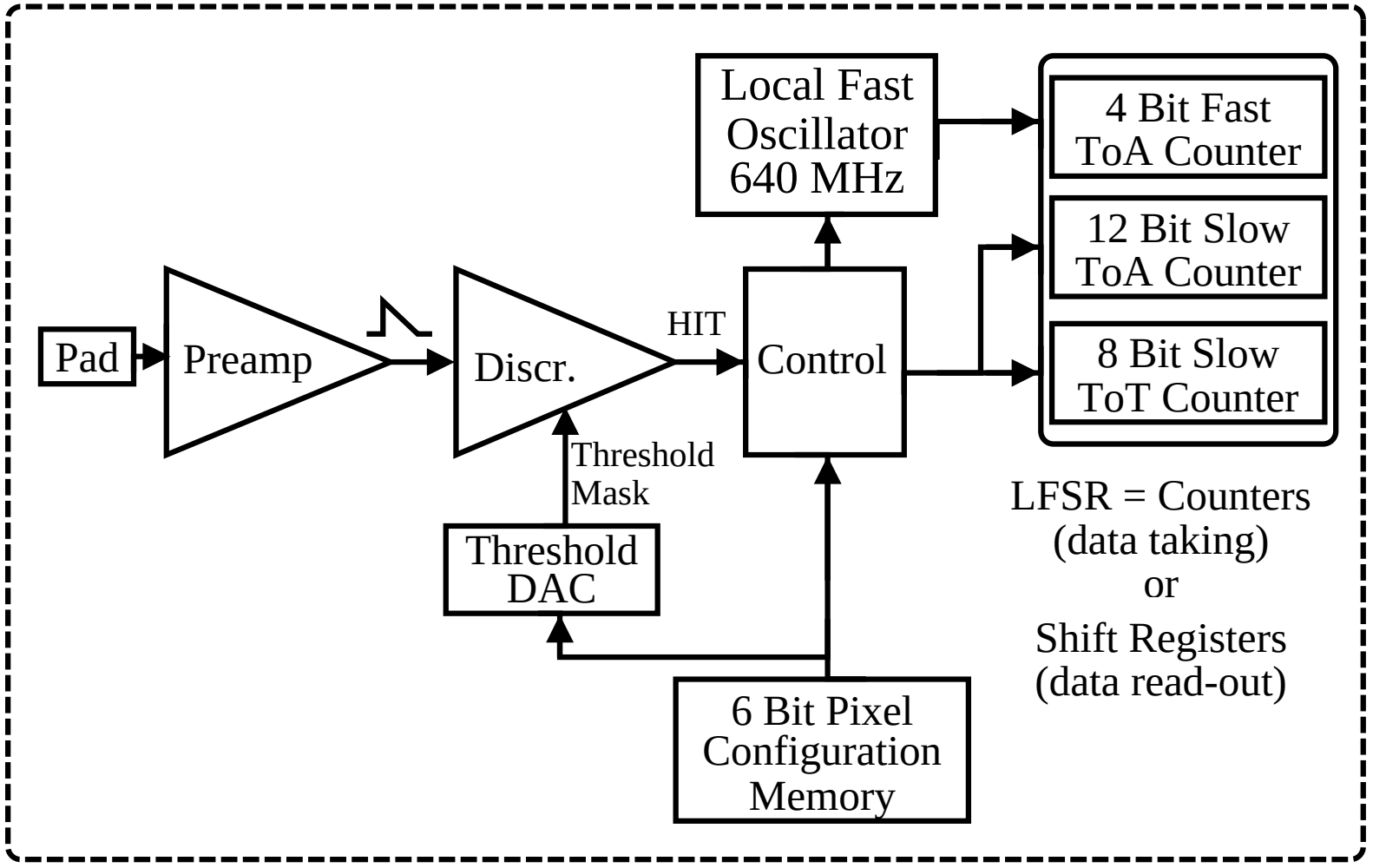


- Particle track image (projection) with 3D track reconstruction
- No sensor leakage current compensation
- Low parasitic capacitance (less than 10fF)
- Single-electron efficiency by high gas gain
- Micro-discharges in avalanche gap
- Time (z-) resolution set by longitudinal diffusion

GOSSIPO-3 Features

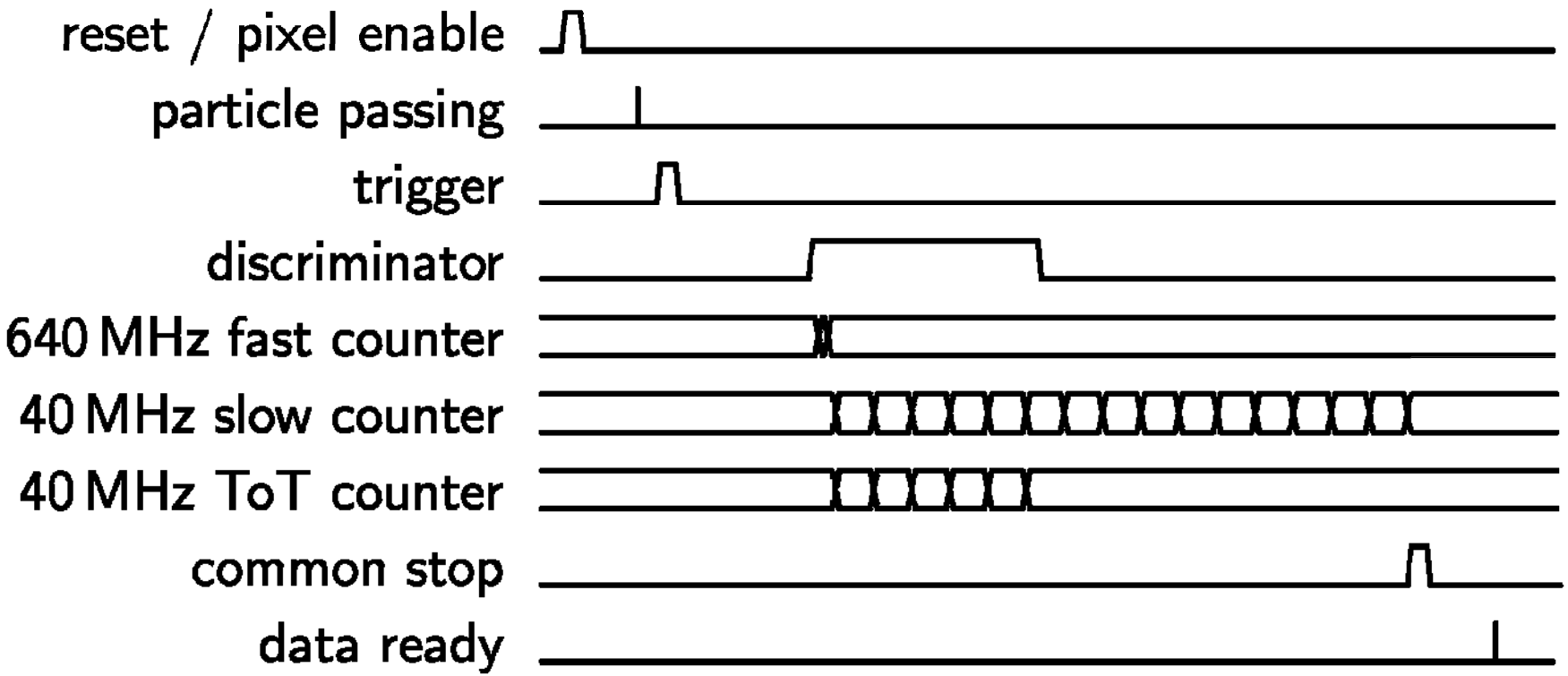
- Small prototype for a read-out chip for MPGDs
- IBM 130nm CMOS (8 metal layers)
- 60μm x 60μm pixels (high granularity)
- ToA Measurement and ToT Measurement [Charge]
- Local TDC in every pixel
- Design Goals:
  - 3μW per channel
  - Arrival time measurement up to 102μs
  - Arrival time accuracy 1.6ns (one fast VCO bin)
  - ToT accuracy 200e^- accuracy (<50ns)

Pixel Electronics



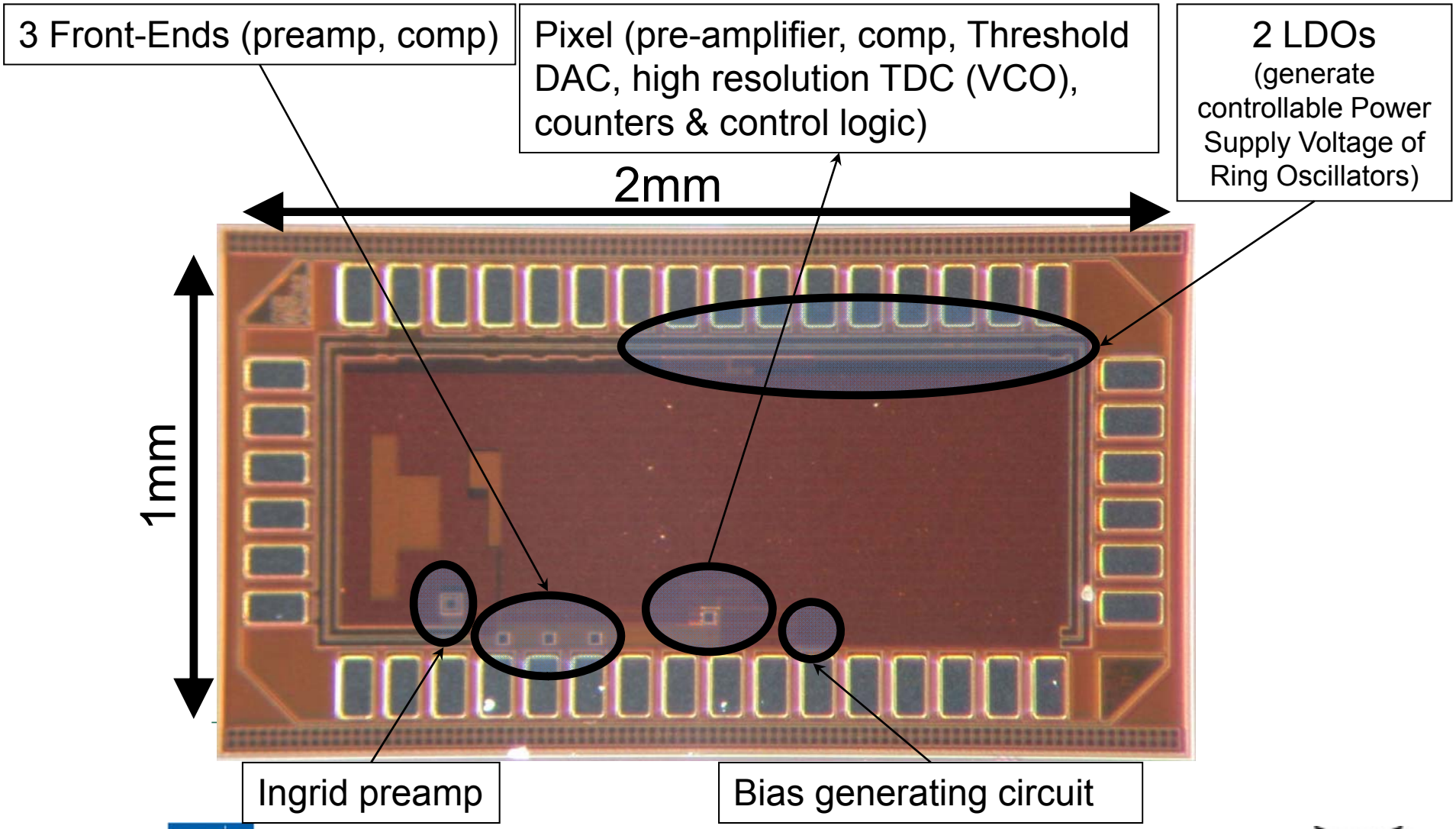
Control Signals:
-Common Stop -Reset -Clock -Token

Common-Stop Timing Scheme

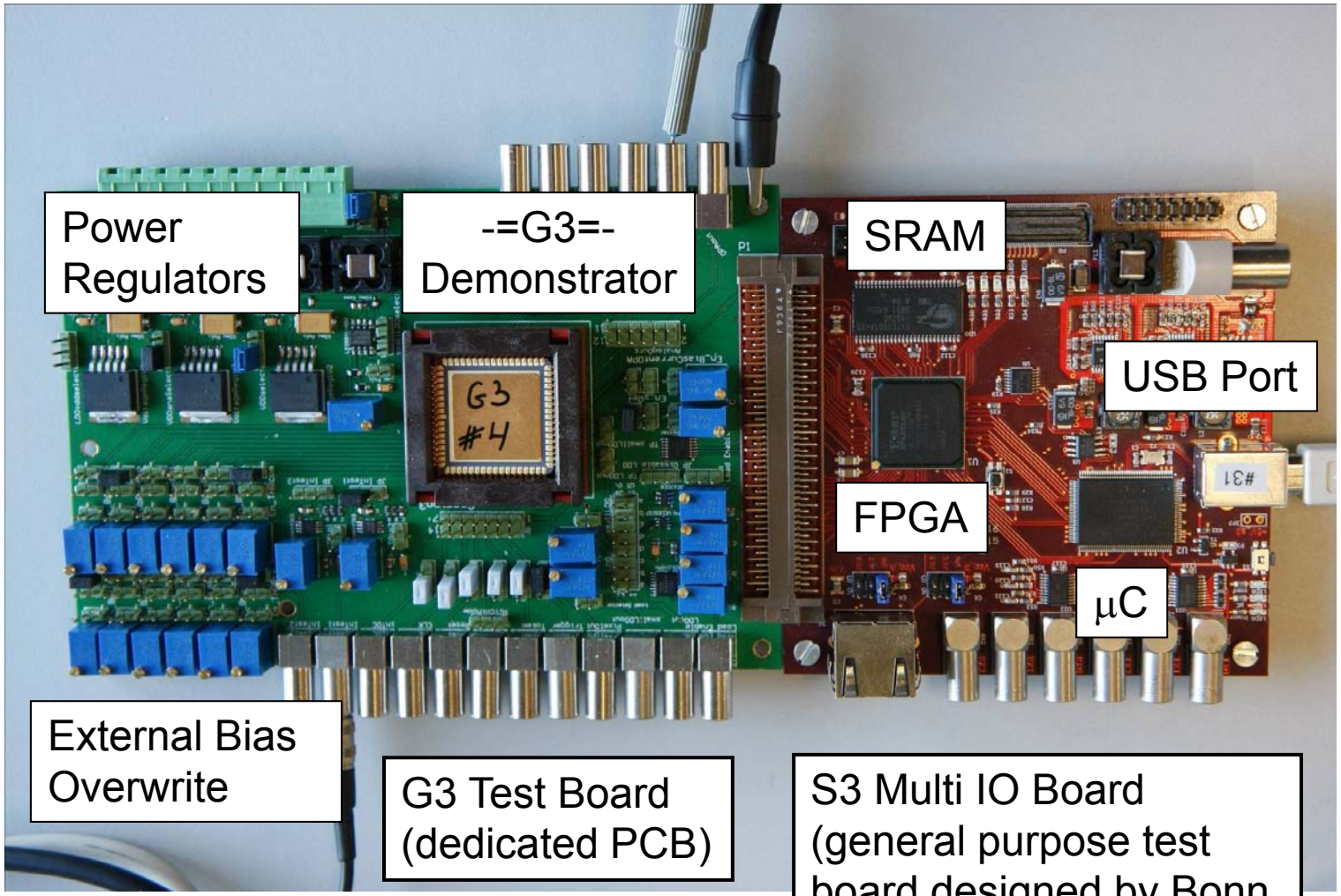


- Fast clock: 640MHz (1.6ns time bins), started by discriminator
- Slow clock: 40MHz (25ns time bins), absolute external timing

GOSSIPO-3 Architecture

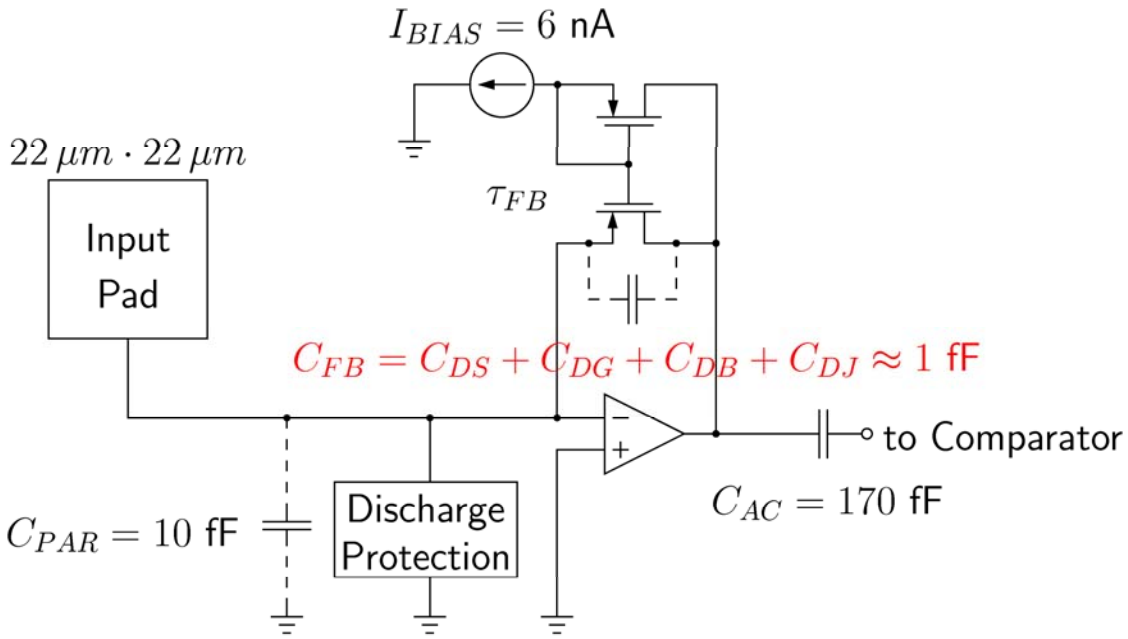


Demonstrator Test Set-Up

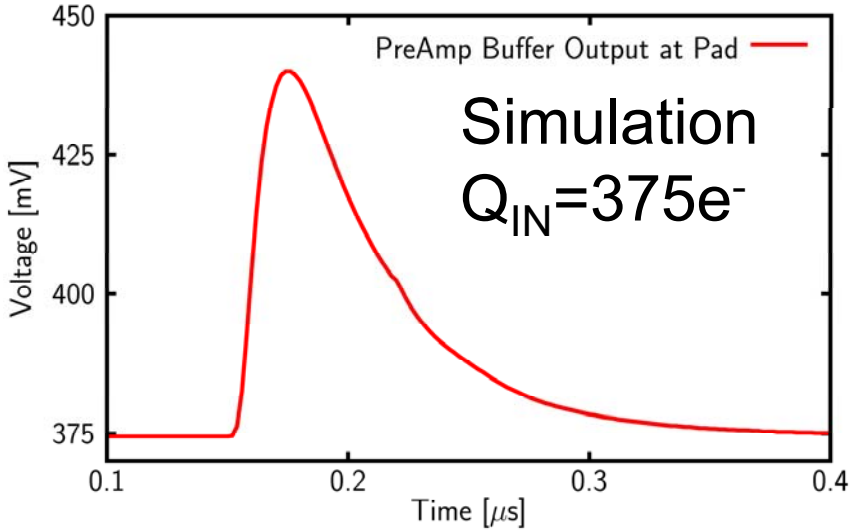


Front-End Performance

- Pre-Amplifier with MOSFET feedback parasitic capacitance
- C_{FB} about 1fF – high gain
- Low parasitic input capacitance

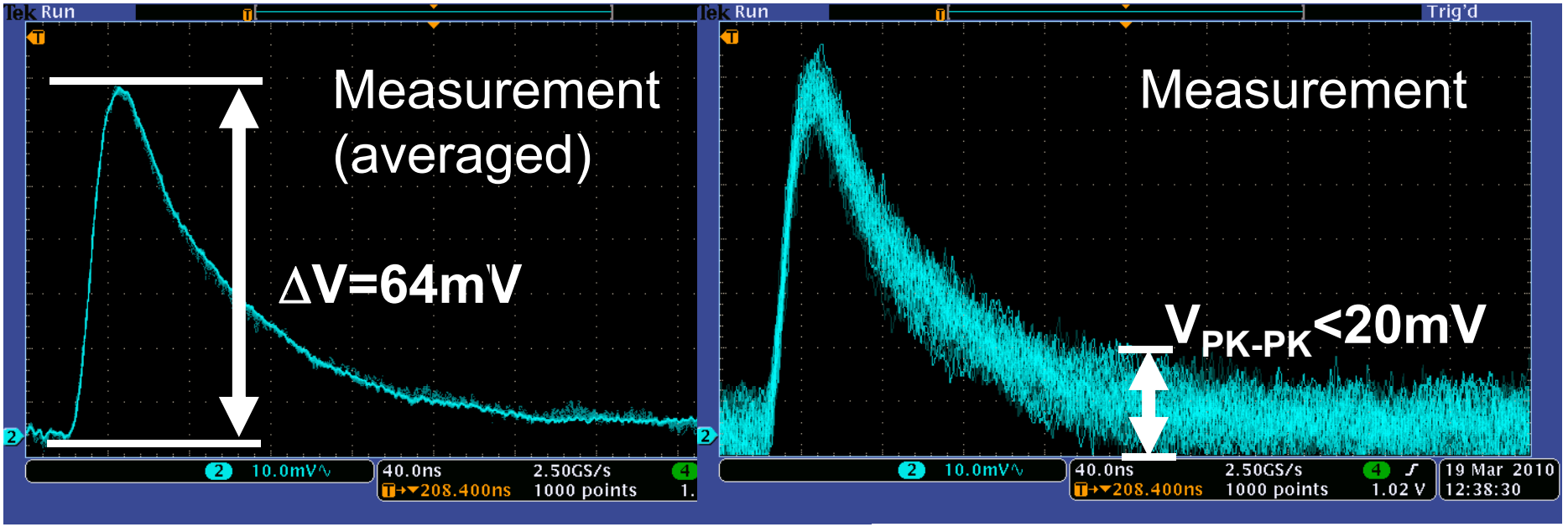


Front-End Performance



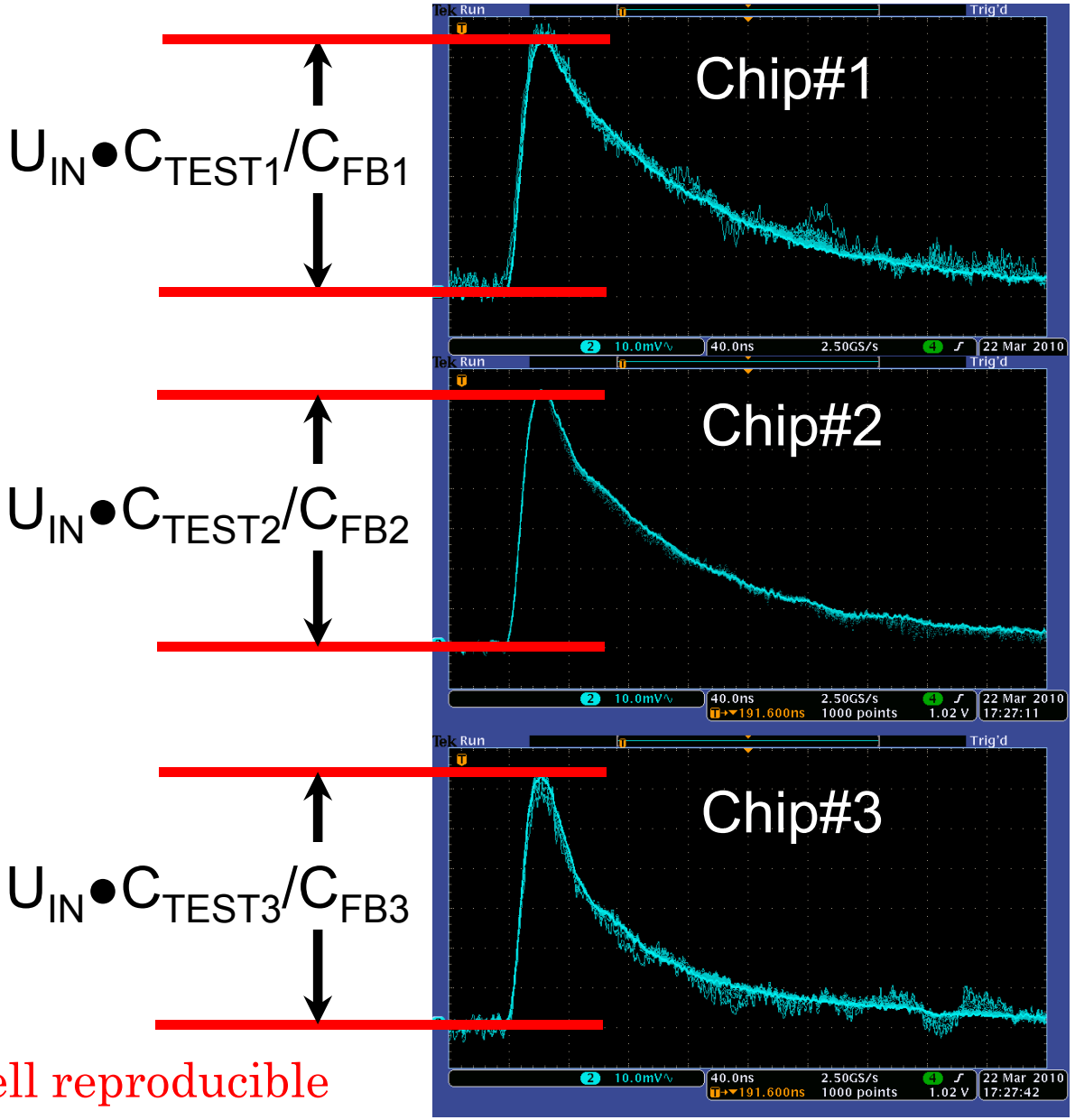
- Excellent pre-amplifier noise performance
  - Charge injection through test pad
  - Measurement includes output pad driver
  - Measured and simulated

    σ_{NOISE} ~ 4mV => ENC ~ 25e$^-$



Front-End Performance

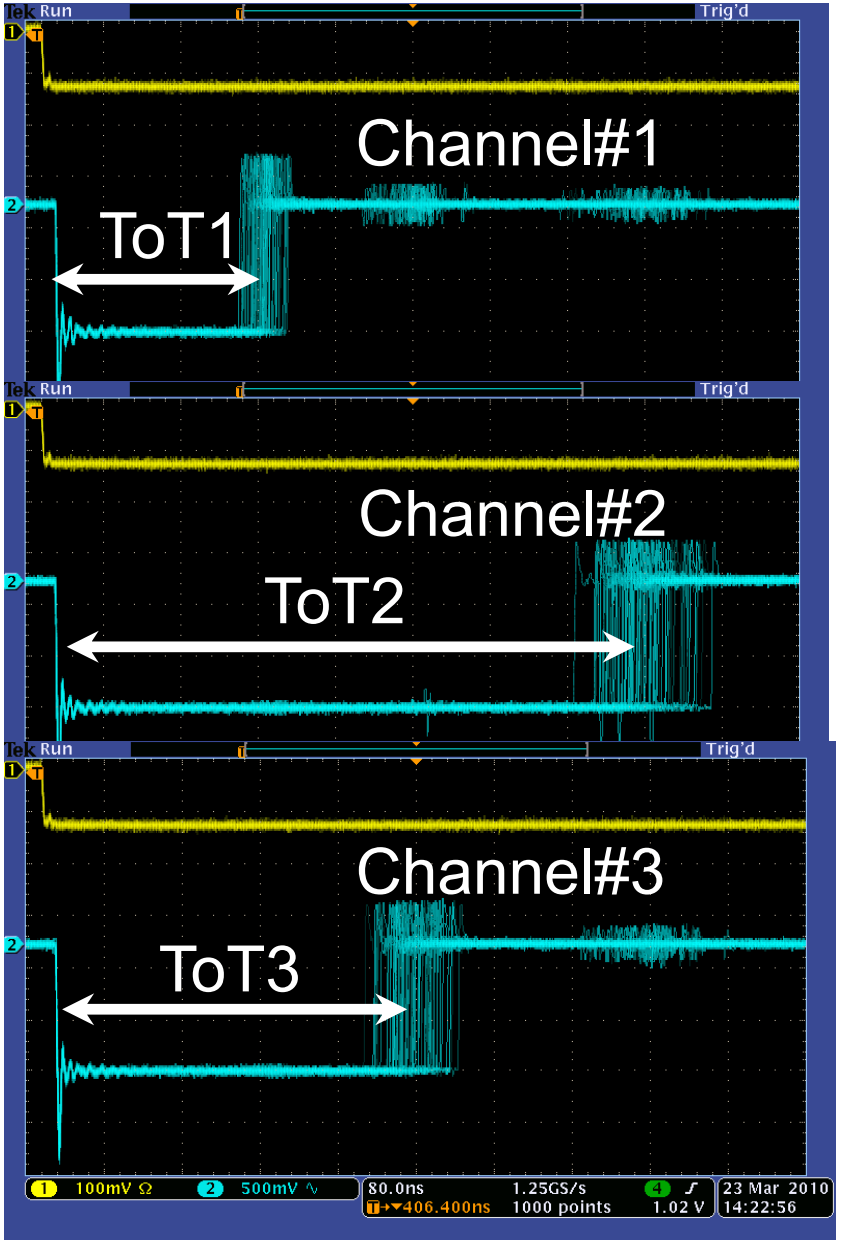
- Pre-amplifer measurement for different channels
  - Metal-Metal Injection Capacitance C_{TEST}~1fF
  - Stable high gain
  - Varying time constant of feedback discharge



C_{TEST} and C_{FB} are well reproducible

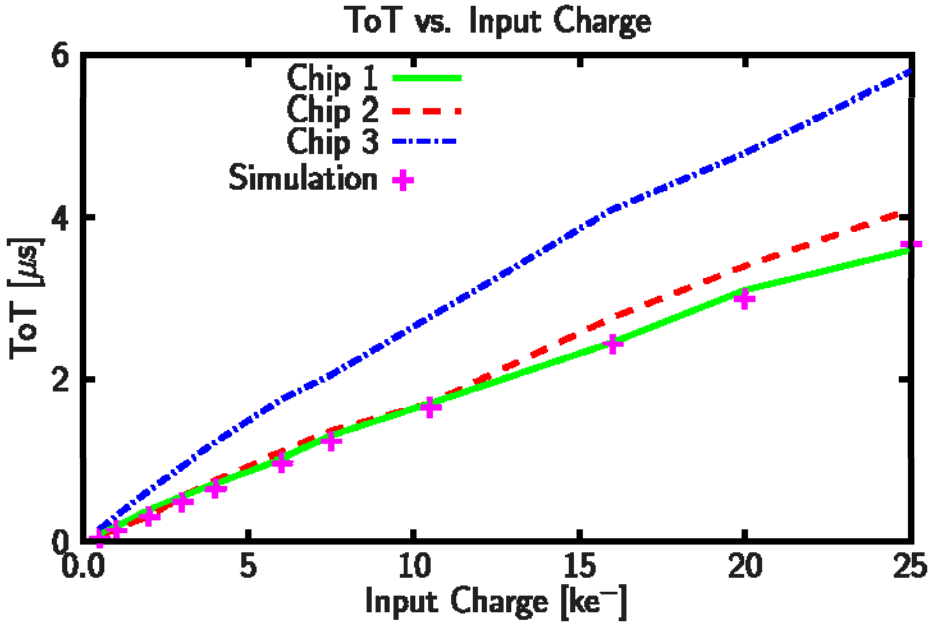
Front-End Performance

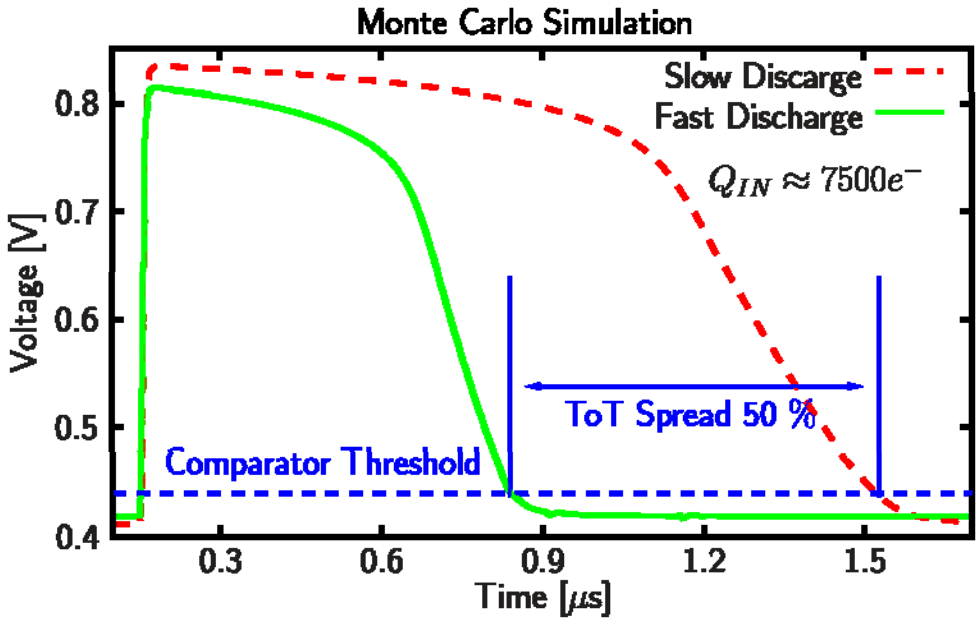
- ToT measurement for different channels
  - Q_{IN}=375e$^-$
  - ToT channel to channel mismatch up to 50% w/o offline calibration
  - Jitter on TOT trailing edge caused by noise on pre-amplifier signal trailing edge
  - Cross-talk between channels observed when pad driver switches



Front-End Performance

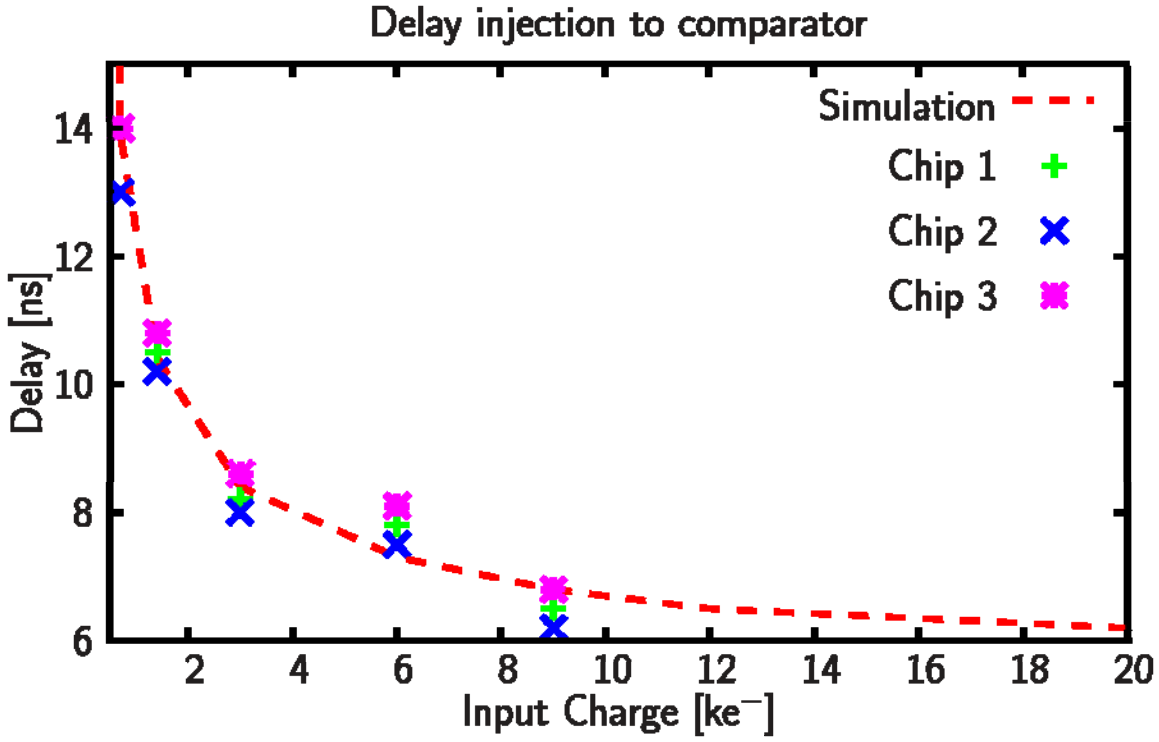
- Analysis of time variation of the feedback discharge
  - Process variation of small feedback MOSFET responsible for variation of feedback current
  - Small feedback MOS needed for high gain





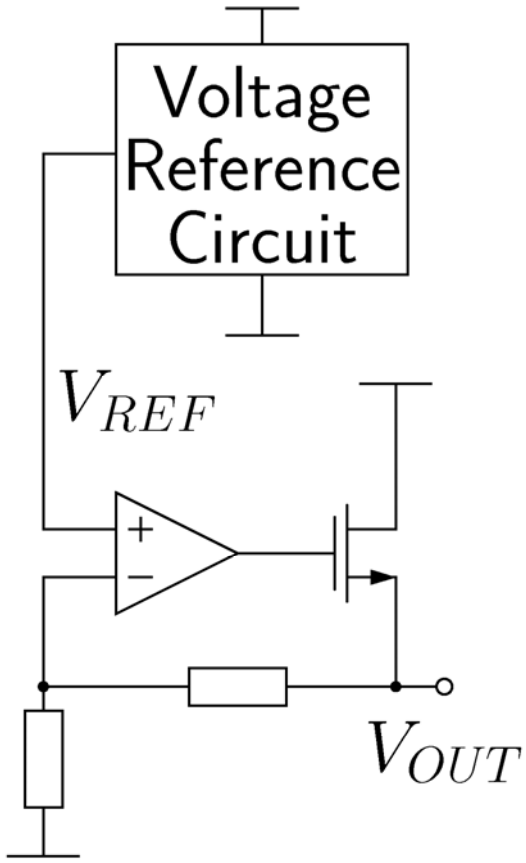
Front-End Performance

- Internal delay [including pad drivers] due to time walk
  - 6ns asymptotical delay for a charge >6000e$^-$
  - Delay injection to comperator >1.6ns TDC bin
  - Further reduction of delay saves offline calibration



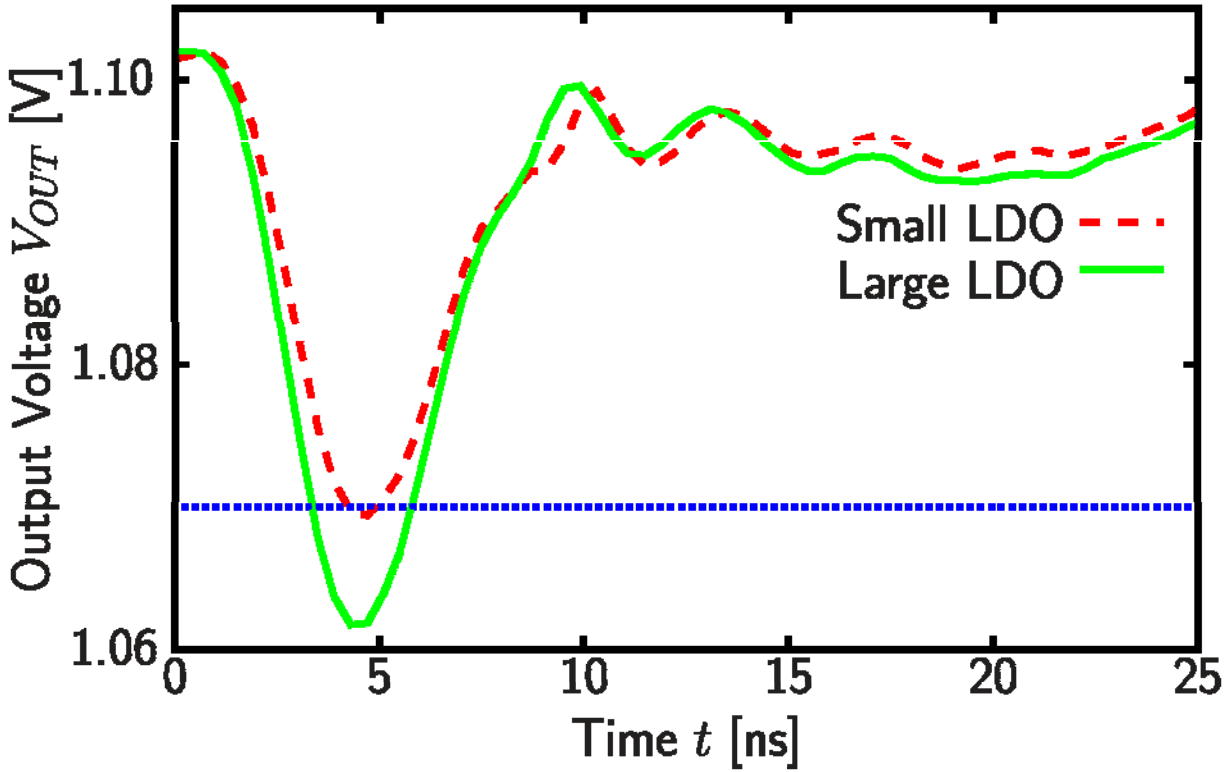
LDO Performance

- LDO controls supply voltage of fast TDC ring-oscillator (arrival time measurement)
- Oscillation frequency of f=640MHz in all process corners
  - Time bin size T=1.56ns
  - Maximum run time 25ns (16 bins)
  - V_{OUT_LDO}=0.61V (fast corner)..1.10V (slow corner)
  - Occupancy expectation gives
    - avg. ΔI_{OUT_LDO}=24mA
    - peak ΔI_{OUT_LDO}=44mA
  - VCO control characteristic allows for max. ΔV_{LDO_OUT}=31mV for 25ns



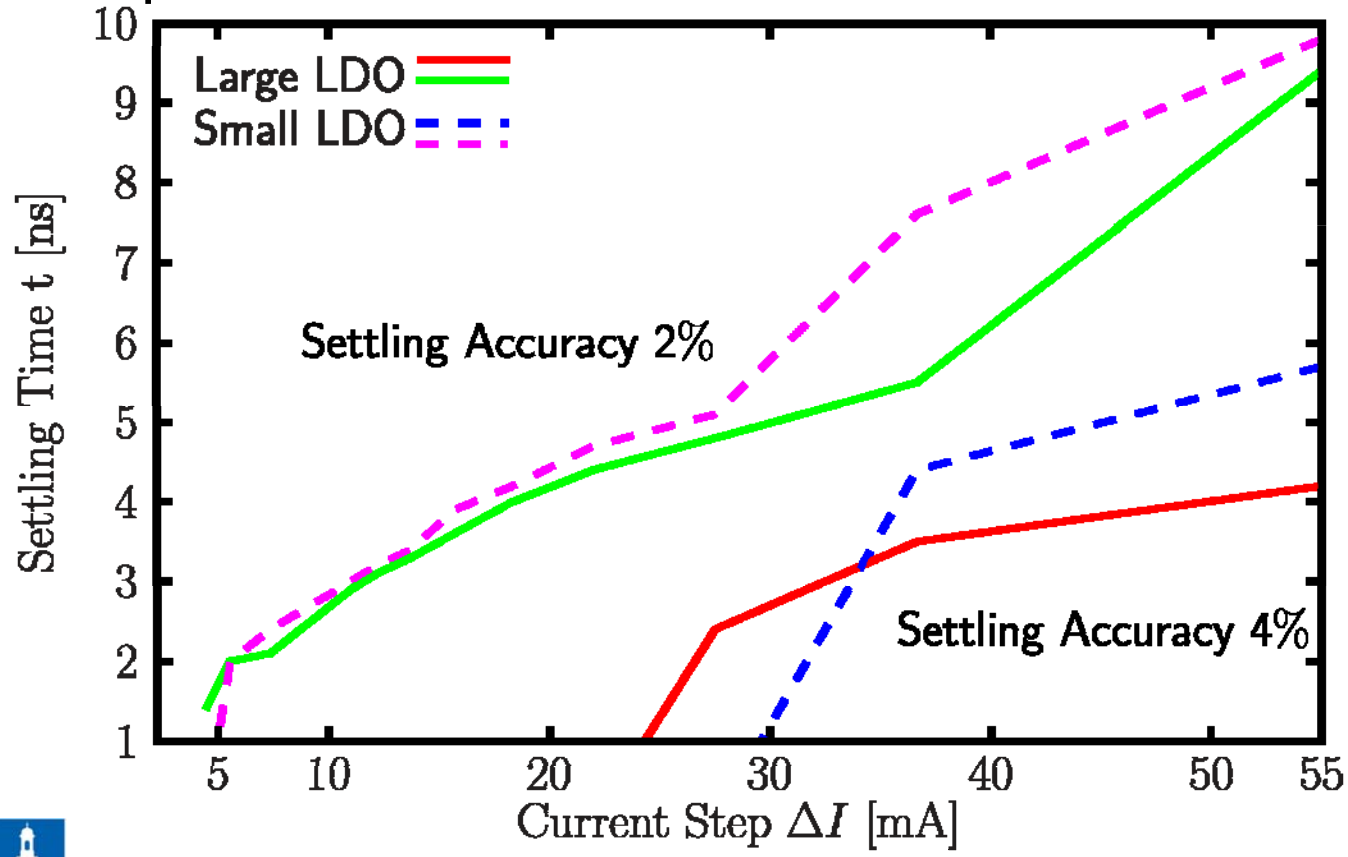
LDO Performance

- Step response to typical load step of 20mA
  - Load externally connected
  - Inductance of package and bond wires limits response time



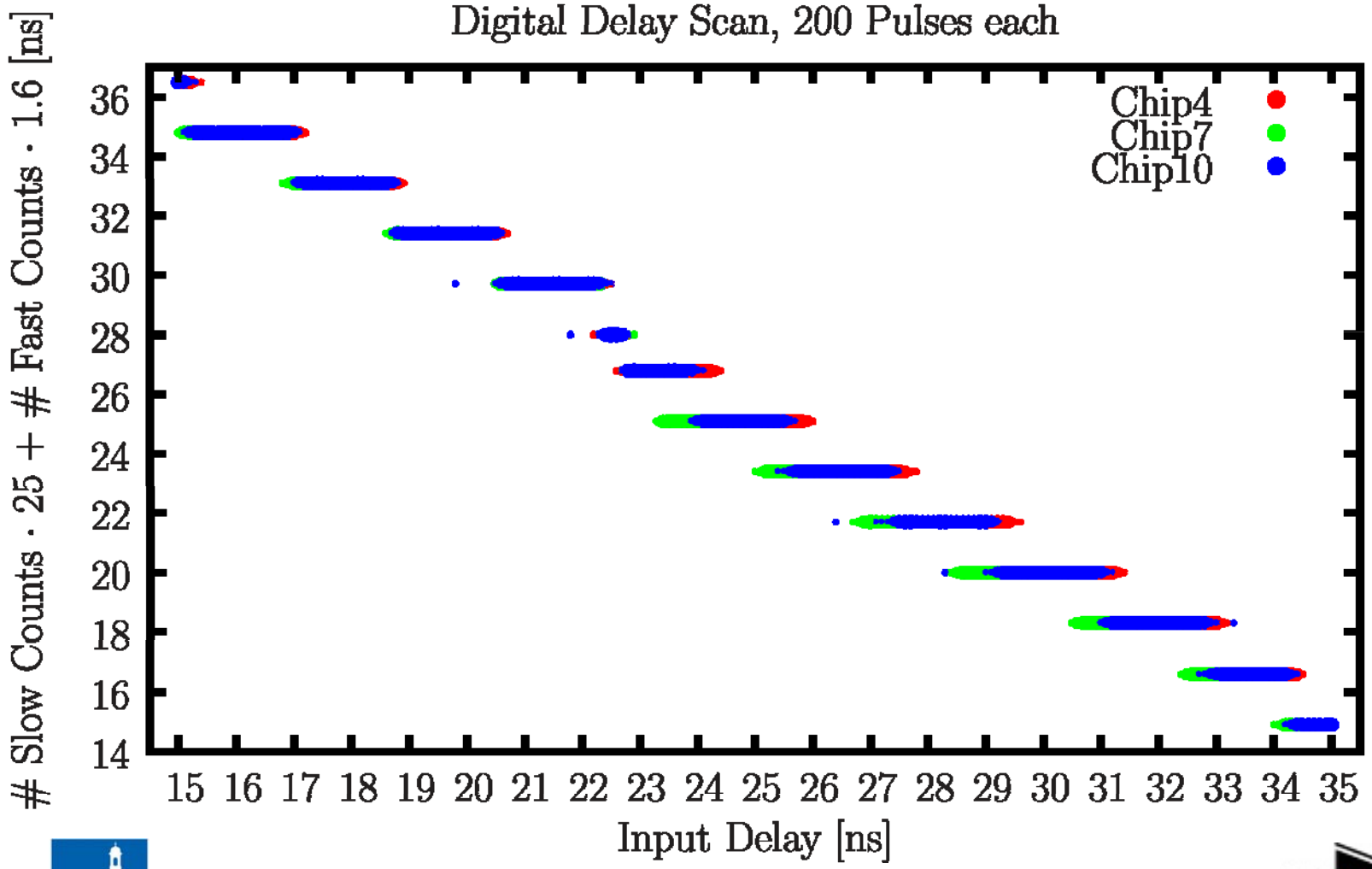
LDO Performance

- Settling time to nominal V_{OUT} value for different (external) load steps



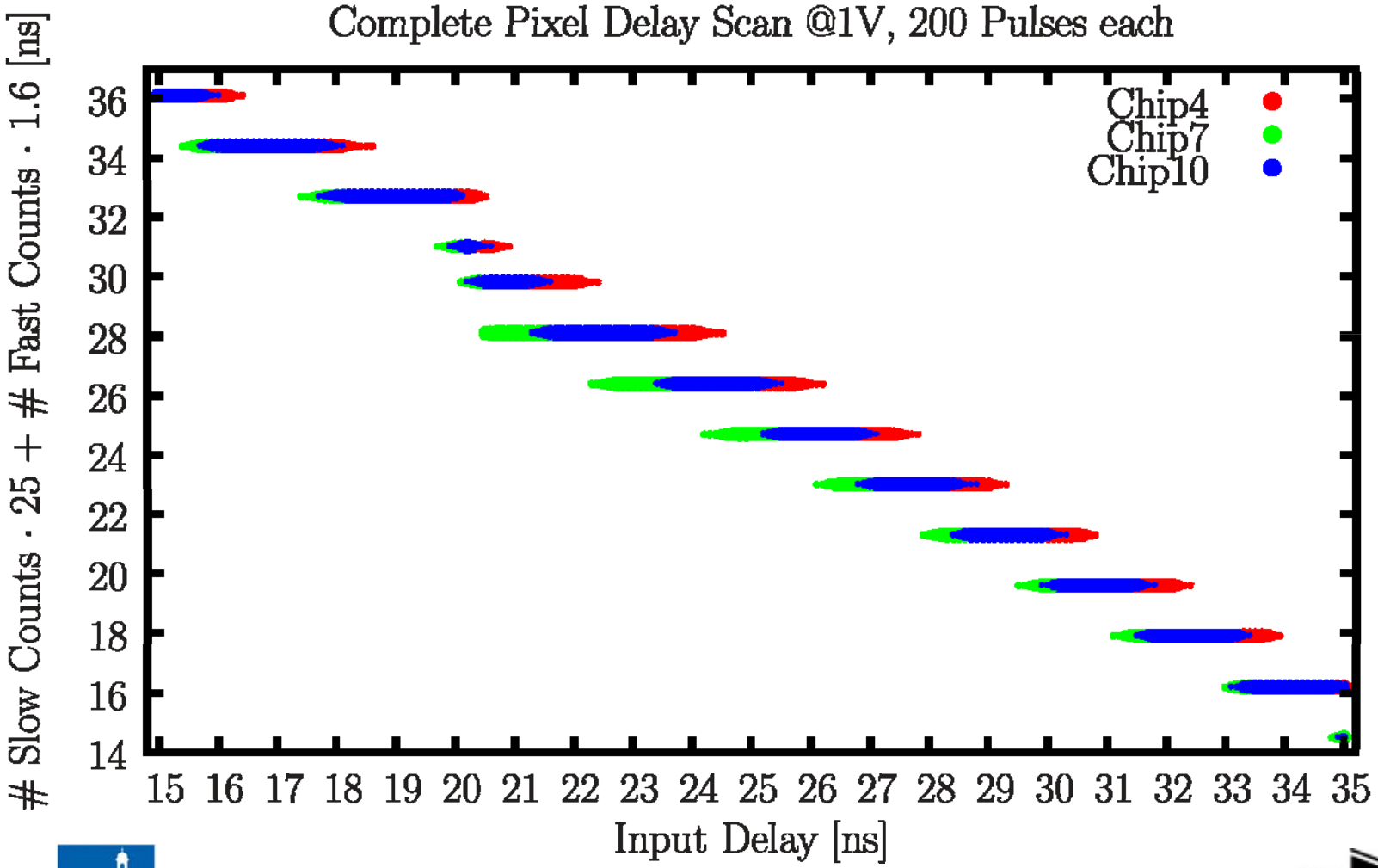
TDC Performance

- Counting steps of TDC (input signal directly at digital logic)



Pixel Performance

- Counting steps of TDC (input signal at analog input)



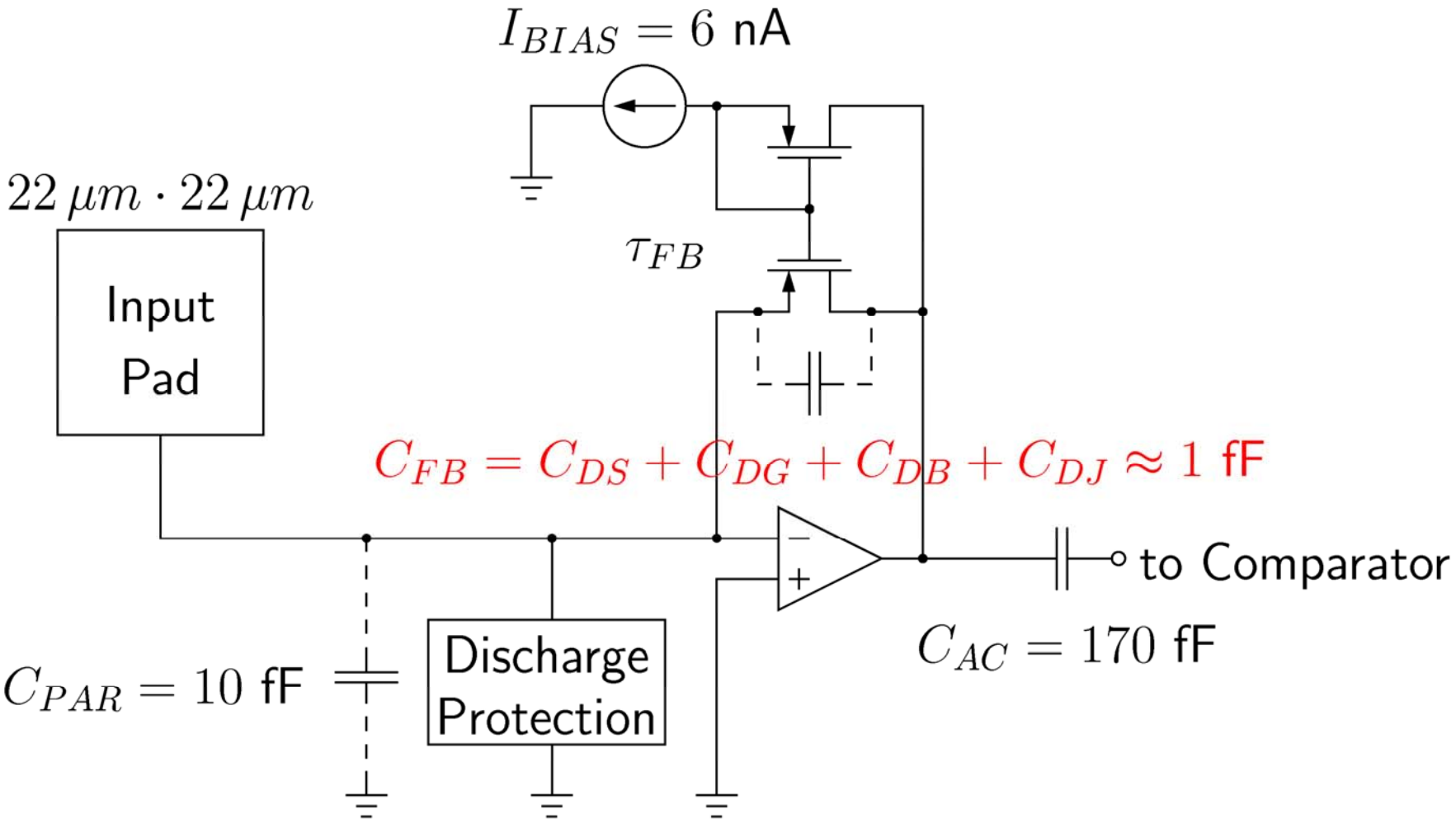
Summary

- Successful operation and measurements:
- Front-End:
  - Internal delay limited by pad drivers
  - Source of pixel to pixel TOT mismatch identified
  - High gain / low noise
- LDOs:
  - Step response time critical for TDC performance
  - Close match between simulation and measurement
- TDC:
  - Transition region of counting steps ~25% of TDC bin (wc)
  - Bin size / fast oscillator frequency reproducible for multiple channels and chips
- Gossipo-3 design team joins Timepix II design efforts
  - Timepix II will benefit from lessons learned

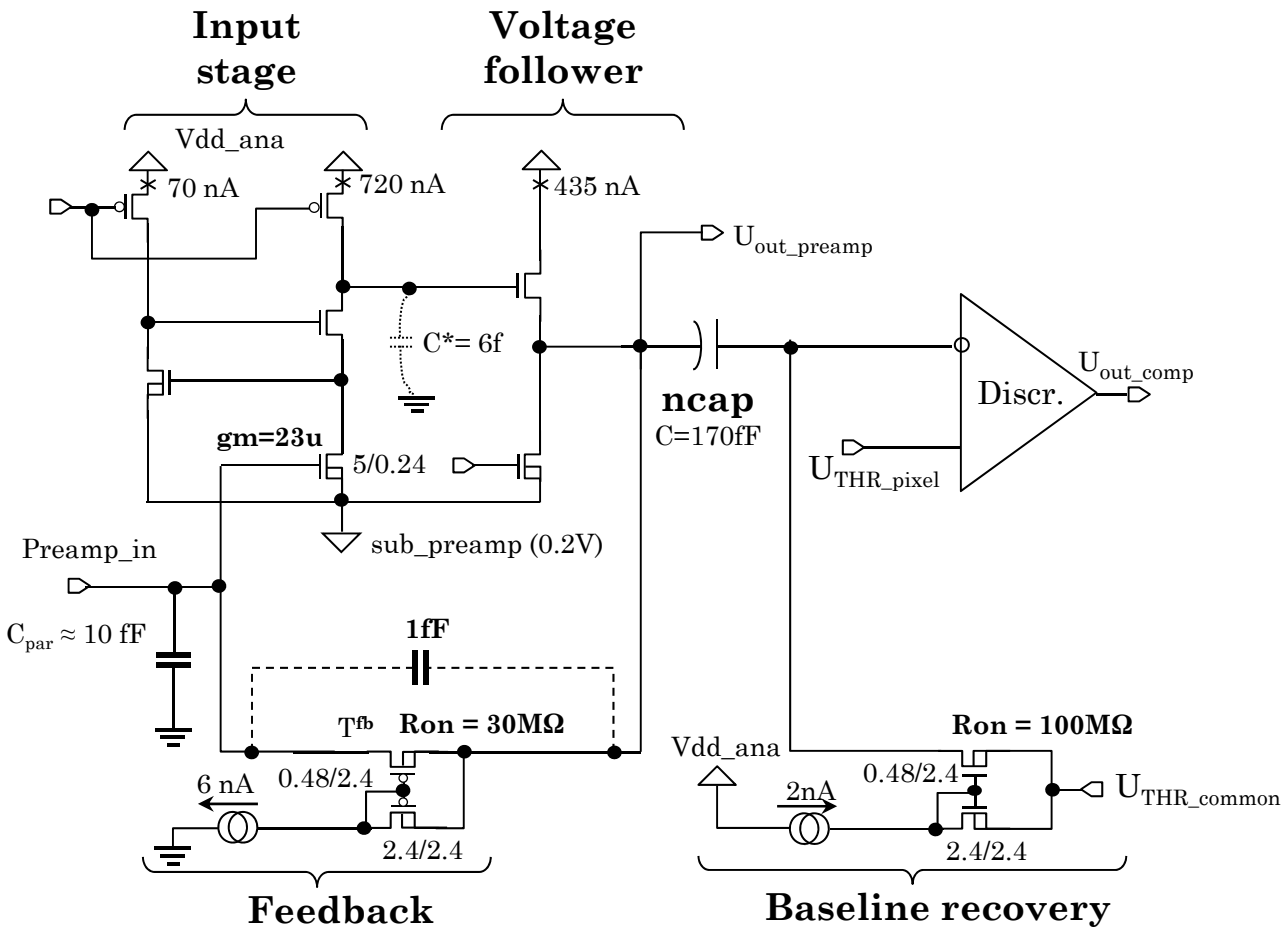
Thanks for your attention!

Backup Slides

Pre-Amplifier Schematic

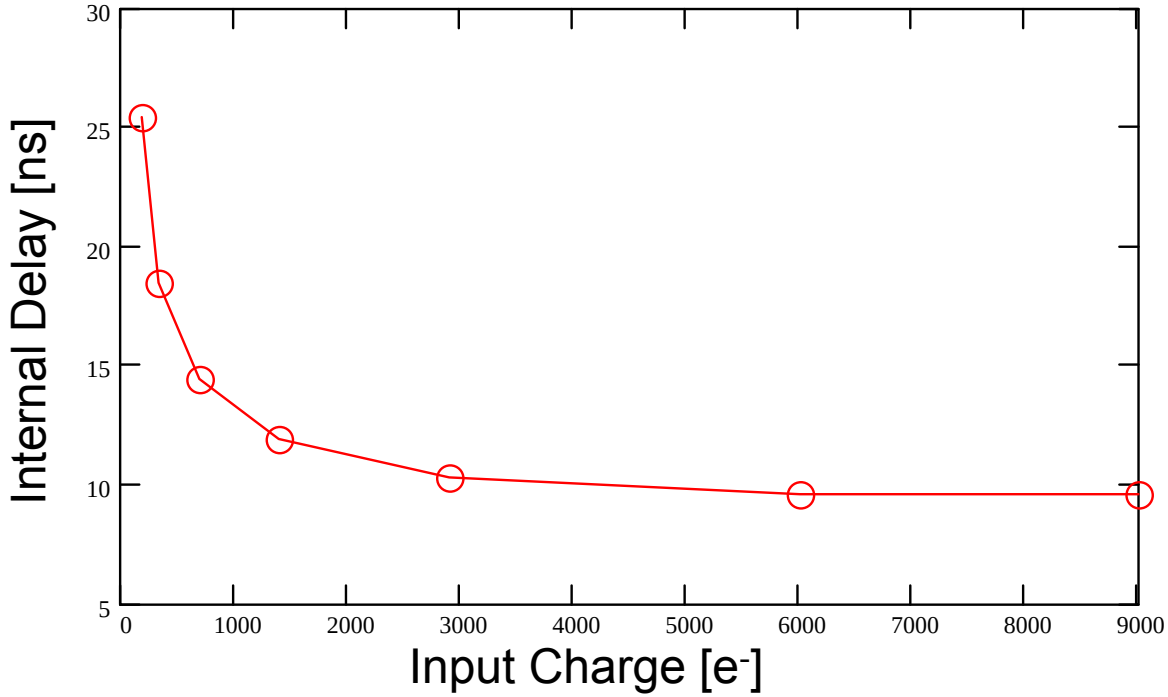


Pre-Amplifier Schematic



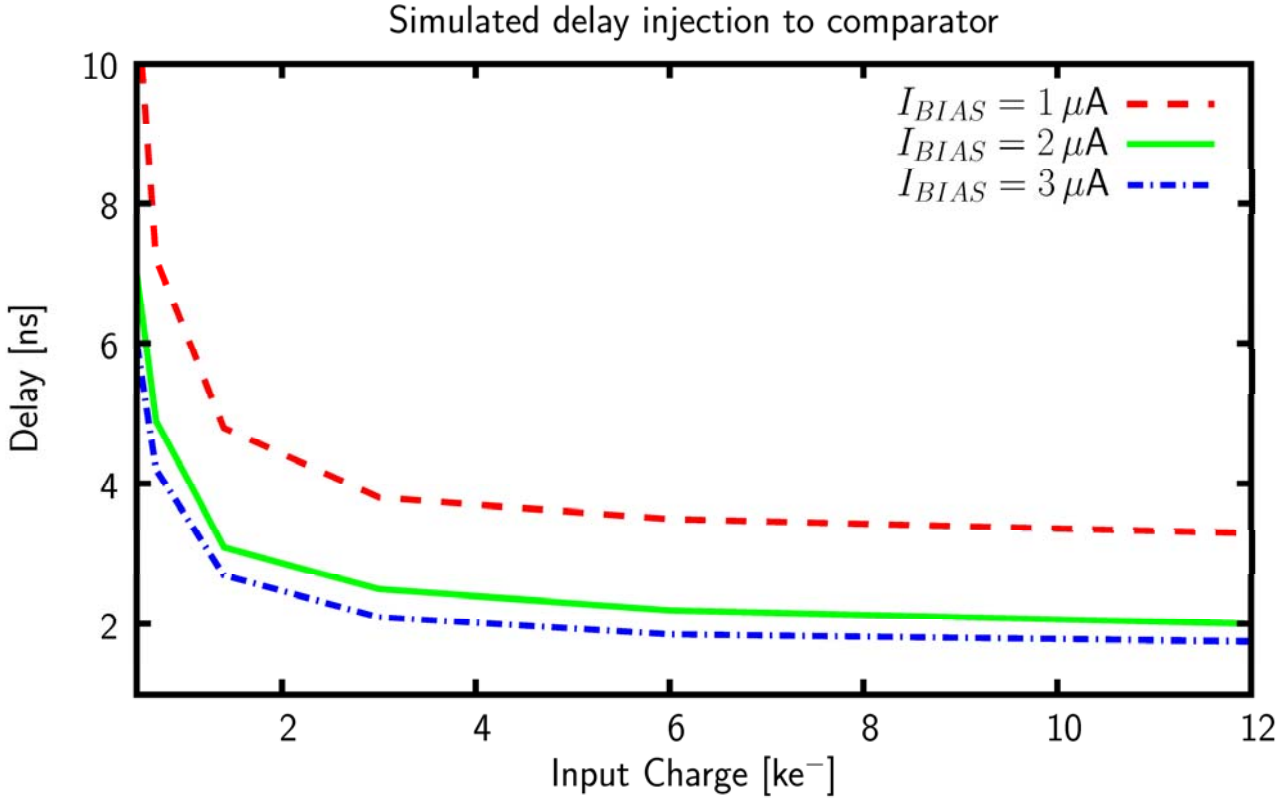
Front-End Performance

- Internal delay (very first measurements)
- 9ns assumptotical delay for a charge >6000e$^-$ (injection to comperator) > 1.6ns TDC bin
- Further reduction of delay needed



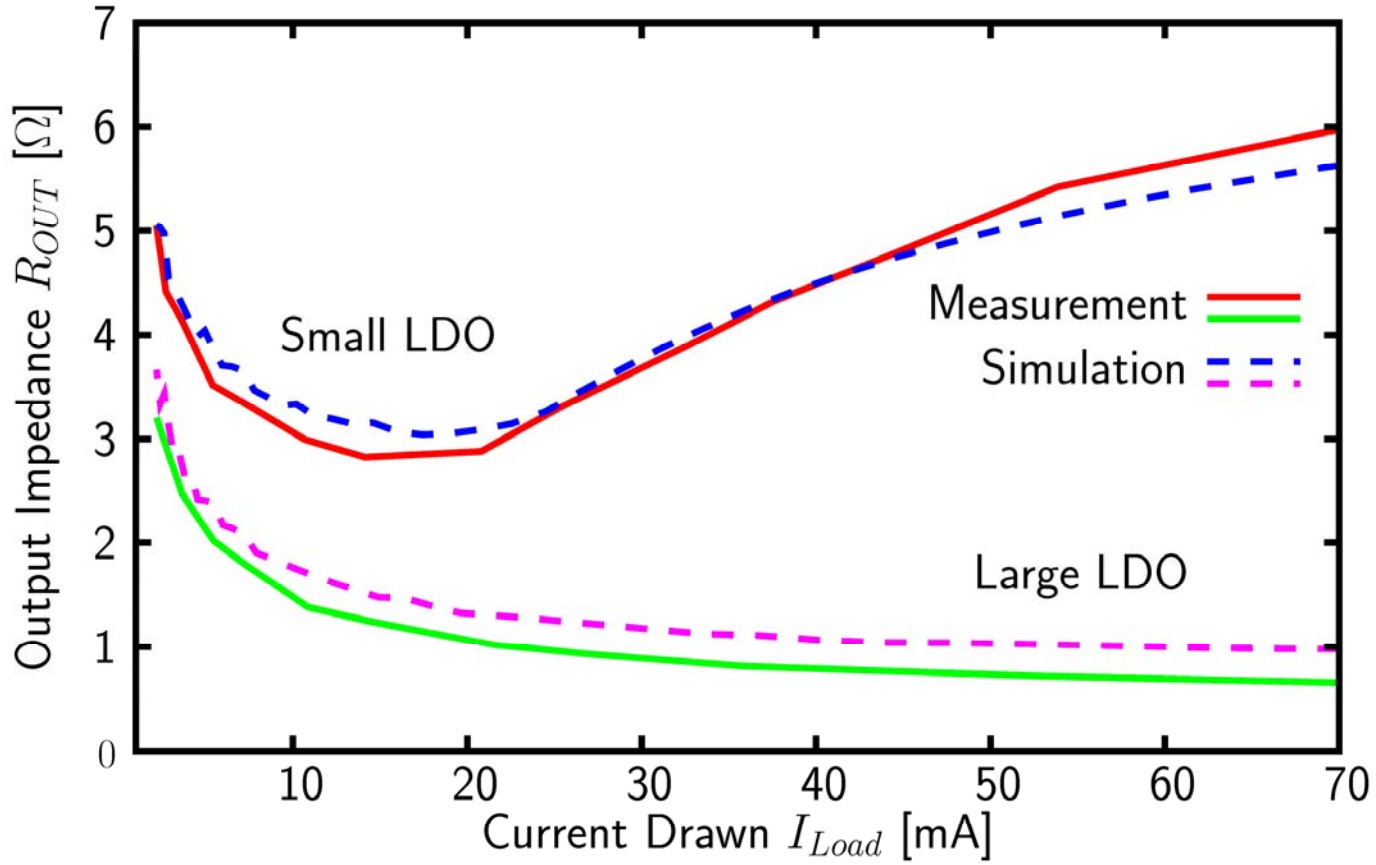
Front-End Performance

- Simulated internal delay [Injection to Comparator Output] based on parasitc extraction



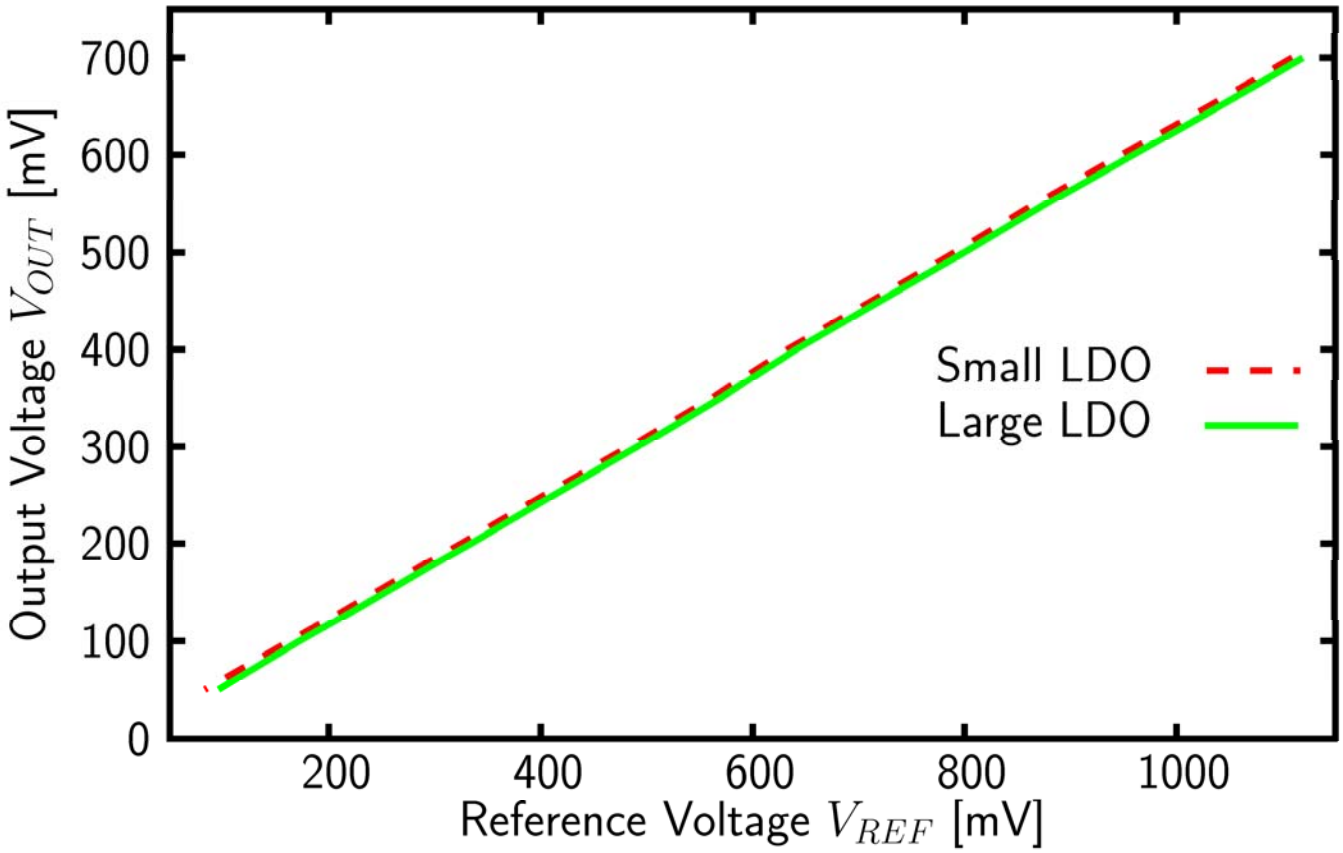
LDO Performance

- Static R_{OUT} measurement



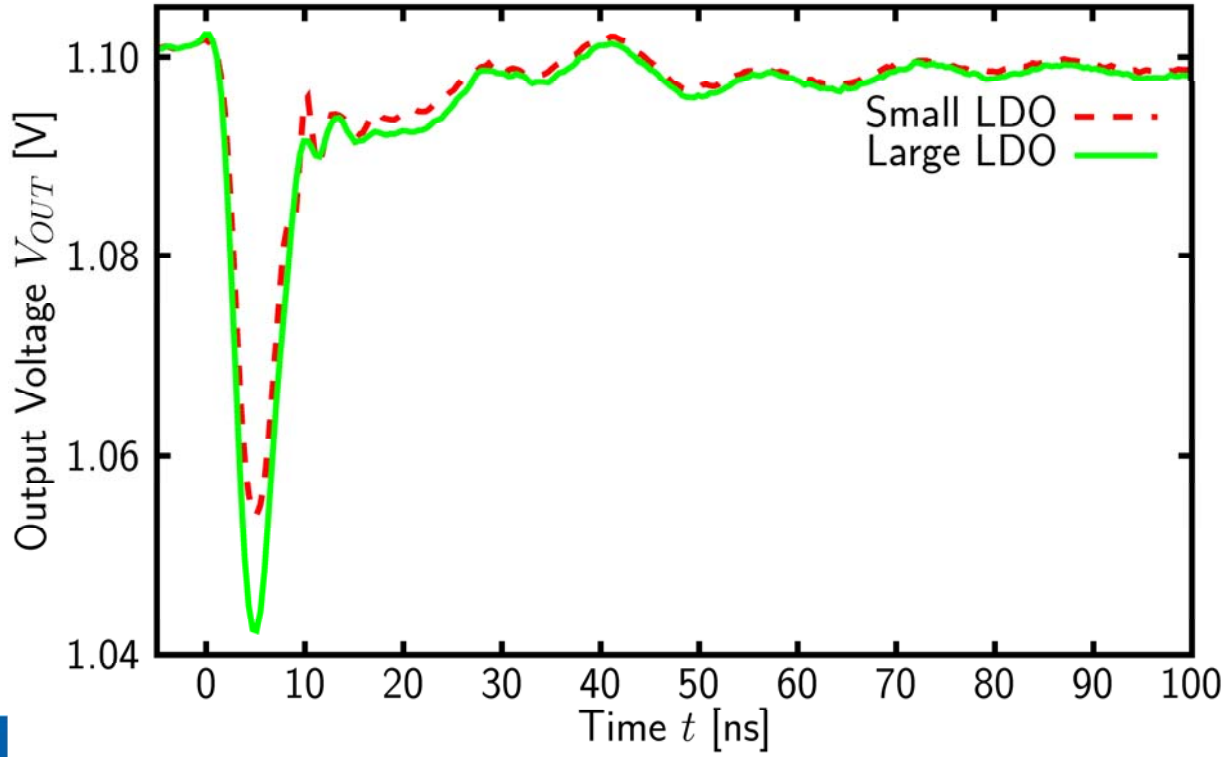
LDO Performance

- Linearity measurement



LDO Performance

- Step response to maximum load step 40mA
  - additional external load
  - inductance of package and bond wires limit response time

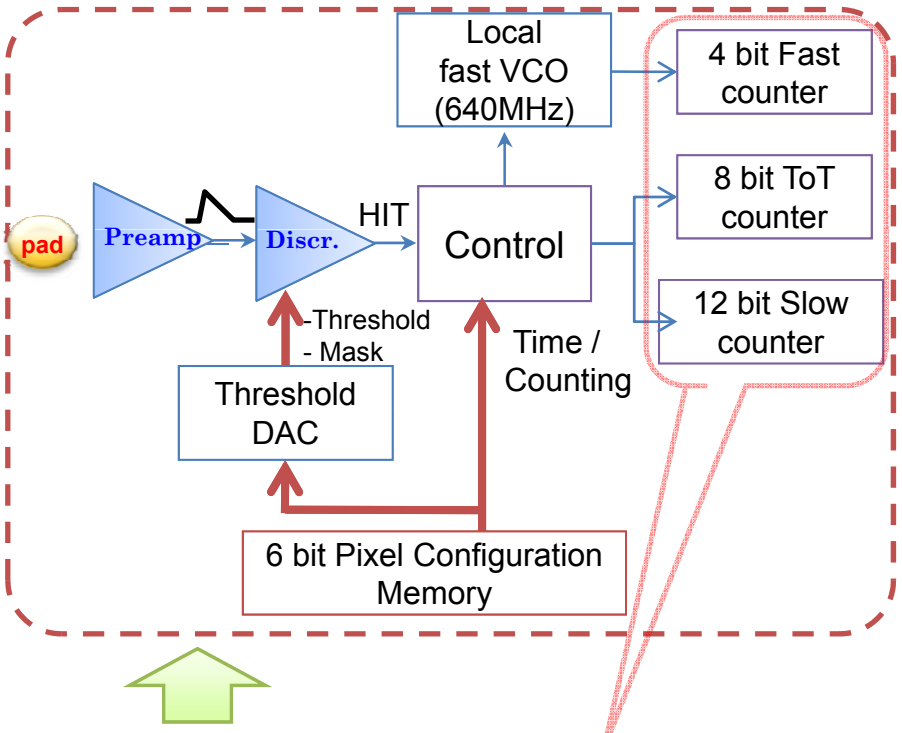


GOSSIP vs. TPC

- GOSSIP
  - Small drift gap (1mm)
  - Track perpendicular to read-out plane
- TPC
  - Large drift gap (1m)
  - Track parallel to read-out plane

Pixel Electronics

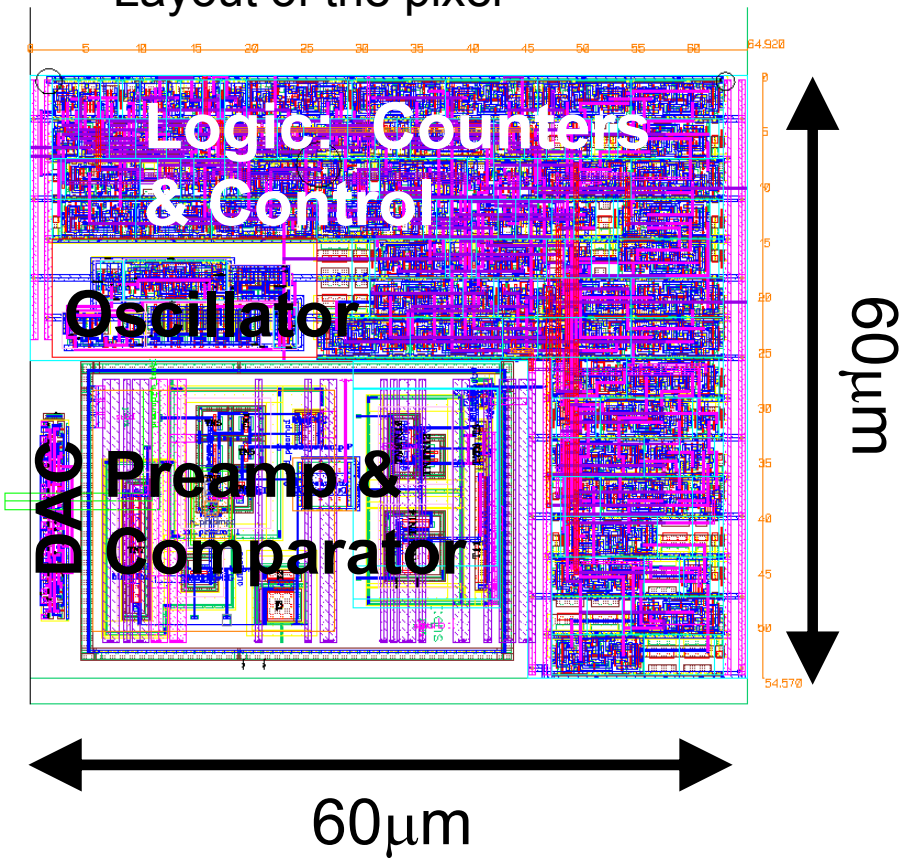
Block diagram of the pixel



Control signals
- Clock
- TRIGGER (common stop)
- TOKEN
- RESET

LFSR = Counters
(data taking)
or
LFSR = Shift registers
(data read-out)

Layout of the pixel



Outlook

- Larger pixel array needed for InGrid test
- The Gossipo-3 design team joins Timepix II design efforts